COM506 Computer Design

Lucida Simulation with ISIM

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This simple tutorial guides you how to run Lucida Platform simulation using ISIM on Linux

- ISIM is ISE-integrated simulator from Xilinx

1. Extract `LucidaPlatform_Virtex5.tar.gz` on Linux
   - `fun_sim` directory is where you run simulation
     i. It includes `testbench.v`
   - `rtl` directory is where **Lucida Platform** lives
     i. The **Lucida Platform** includes icore, cache, mmu, I/O devices. Those devices are synthesizable.
   - Env directory is where functional device models live only for simulation
     i. The device models are connected to the Lucida Platform for simulation. They include memory models, UART and so on.

2. Download the ISIM simulation script from
   http://esca.korea.ac.kr/teaching/com506_CD/patch_ISIM.tar.gz
   - Do "**`tar zxvf patch_ISIM.tar.gz`**" at the parent directory of `fun_sim`.

```
suhtw@suhtw-desktop:~/projects/adchips/database/FPGA/LucidaPlatform_Virtex5$ ll
total 40
drwxr-xr-x  2 suhtw suhtw 4096 2012-10-15 16:01 Enc_sim
drwxr-xr-x  4 suhtw suhtw 4096 2012-09-27 09:08 Env
drwxr-xr-x  5 suhtw suhtw 4096 2012-10-15 19:34 fun_sim
-rwxr-xr-x  1 suhtw suhtw 6707 2012-09-26 13:40 :gen_to_user.pl
-rw-r--r--  1 suhtw suhtw  231 2012-09-26 13:40 Makefile
-rw-r--r--  1 suhtw suhtw 2857 2012-10-16 00:06 patch_ISIM.tar.gz
drwxr-xr-x 34 suhtw suhtw 4096 2012-10-15 19:35 rtl
-rw-r--r--  1 suhtw suhtw   76 2012-09-26 16:52 SourceMe
drwxr-xr-x  4 suhtw suhtw 4096 2012-09-27 09:08 syn
suhtw@suhtw-desktop:~/projects/adchips/database/FPGA/LucidaPlatform_Virtex5$ tar zxvf patch_ISIM.tar.gz
./fun_sim/
./fun_sim/vlist_env_ISIM
./fun_sim/vlist_rtl_ISIM
./fun_sim/run_Lucida_ISIM
./fun_sim/SourceMe_ISIM
./rtl/
./rtl/top/
./rtl/top/define_ISIM
suhtw@suhtw-desktop:~/projects/adchips/database/FPGA/LucidaPlatform_Virtex5$
```

3. Make sure that you have the following files in `fun_sim` directory.

```
suhtw@suhtw-desktop:~/projects/adchips/database/FPGA/LucidaPlatform_Virtex5/fun_sim$ ll *ISIM
-rwxr-xr-x 1 suhtw suhtw   154 2012-10-15 19:34 run_Lucida_ISIM
-rw-r--r-- 1 suhtw suhtw    37 2012-10-15 19:34 SourceMe_ISIM
-rw-r--r-- 1 suhtw suhtw   338 2012-10-15 19:34 vlist_env_ISIM
-rw-r--r-- 1 suhtw suhtw 15104 2012-10-15 19:34 vlist_rtl_ISIM
suhtw@suhtw-desktop:~/projects/adchips/database/FPGA/LucidaPlatform_Virtex5/fun_sim$
```

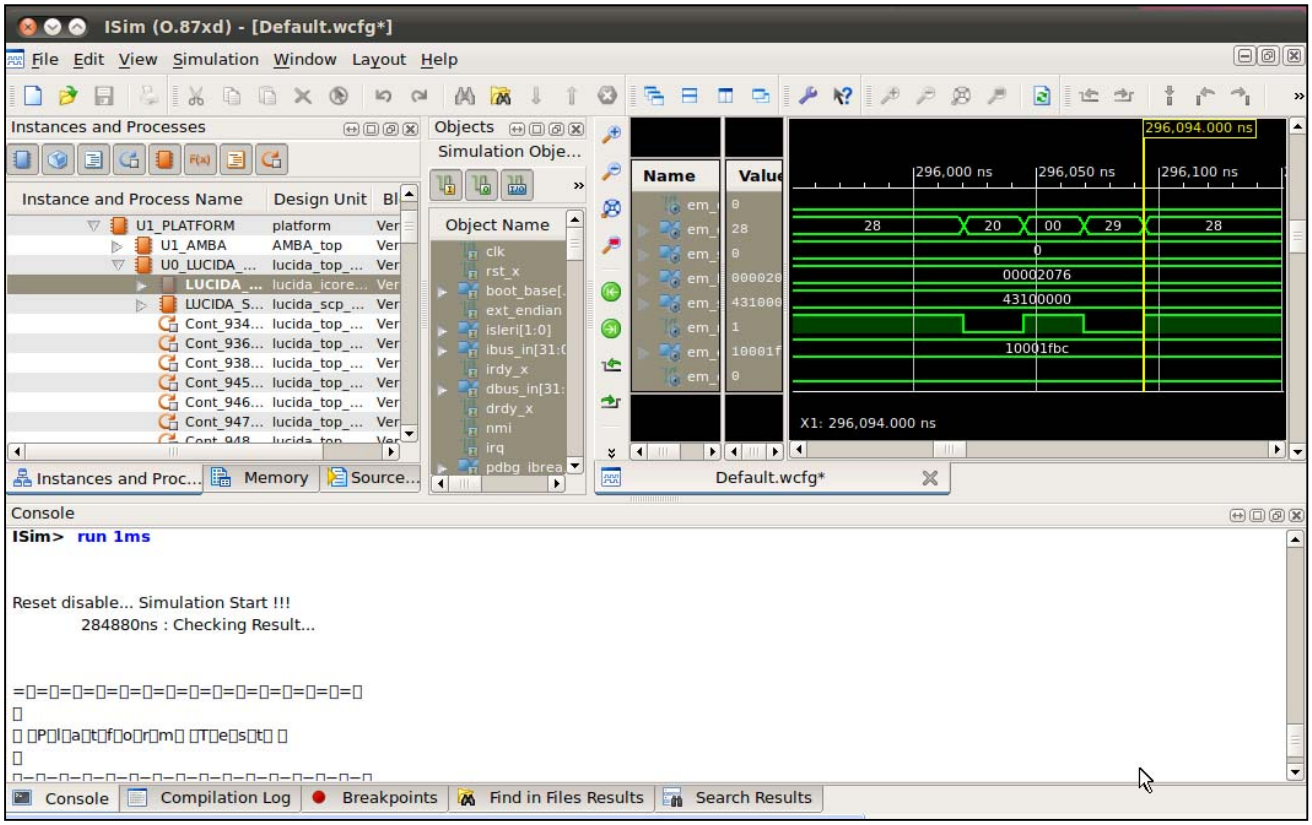
4. Edit SoureMe_ISIM, so that XILINX_ISE points to the ISE installation directory. Then, do "source SourceME_ISIM"

```
suhtw@suhtw-desktop:~/projects/adchips/database/FPGA/LucidaPlatform_Virtex5/fun_sim$ ll *ISIM
-rwxr-xr-x 1 suhtw suhtw   154 2012-10-15 19:34 run_Lucida_ISIM
-rw-r--r-- 1 suhtw suhtw    37 2012-10-15 19:34 SourceMe_ISIM
-rw-r--r-- 1 suhtw suhtw   338 2012-10-15 19:34 vlist_env_ISIM
-rw-r--r-- 1 suhtw suhtw 15104 2012-10-15 19:34 vlist_rtl_ISIM
suhtw@suhtw-desktop:~/projects/adchips/database/FPGA/LucidaPlatform_Virtex5/fun_sim$ more SourceMe_ISIM
export XILINX_ISE=/home/suhtw/Xilinx
suhtw@suhtw-desktop:~/projects/adchips/database/FPGA/LucidaPlatform_Virtex5/fun_sim$ ll /home/suhtw/Xilinx
total 4
drwxr-xr-x 8 root root 4096 2012-10-07 16:50 ISE_DS
suhtw@suhtw-desktop:~/projects/adchips/database/FPGA/LucidaPlatform_Virtex5/fun_sim$ source SourceMe_ISIM
```

5. Run "run_Lucida_ISIM". The batch file compiles the **Lucida Platform** and function device models, generate the simulation executable, Sim_Lucida, and start simulation

```
suhtw@suhtw-desktop:~/projects/adchips/database/FPGA/LucidaPlatform_Virtex5/fun_sim$ ./run_Lucida_ISIM
Running: /home/suhtw/Xilinx/ISE_DS/ISE/bin/lin64/unwrapped/fuse -f ../rtl/top/define_ISIM -prj vlist_rtl_ISIM -f
 vlist_env_ISIM -o Sim_Lucida work.testbench work.glbl
ISim O.87xd (signature 0x8ddf5b5d)
Number of CPUs detected in this system: 8
Turning on mult-threading, number of parallel sub-compilation jobs: 16
```

- Add any signal you want to observe and do "run 1ms"
    i. You'll see some message (Platform Test) coming up
- I think you need to replace TEST_1024bit.rom in fun_sim directory for simulation of your program; <- it seems not a correct statement.



Dhrystone simulation with ISIM: The difference in hardware is an increase of DSPM (Data Scratchpad Memory) size to 32KB (the previous platform had a 8KB DSPM) and software (spsram_16kx32_Ben_init.mif).

- Do the following between step 3 and step 4 on page 1:
  - Download http://esca.korea.ac.kr/teaching/com506_CD/patch_ISIM_Dhrystone.tar.gz
  - Do "**`tar zxvf patch_ISIM_Dhrystone.tar.gz`**" at the parent directory of `fun_sim`.

```
suhtw@suhtw-desktop:~/projects/adchips/database/FPGA/LucidaPlatform_Virtex5_ISIM_Dhrystone$ tar zxvf patch_ISIM_Dhrystone.tar.gz
fun_sim/
fun_sim/vlist_env_ISIM
fun_sim/spsram_16kx32_Ben_init.mif
rtl/
rtl/top/
rtl/top/top.v
rtl/top/platform.v
rtl/top/define_ISIM
suhtw@suhtw-desktop:~/projects/adchips/database/FPGA/LucidaPlatform_Virtex5_ISIM_Dhrystone$
```

- You should be able to see the messages from Dhrystone shown below in step 5.