COMP212 Computer Architecture

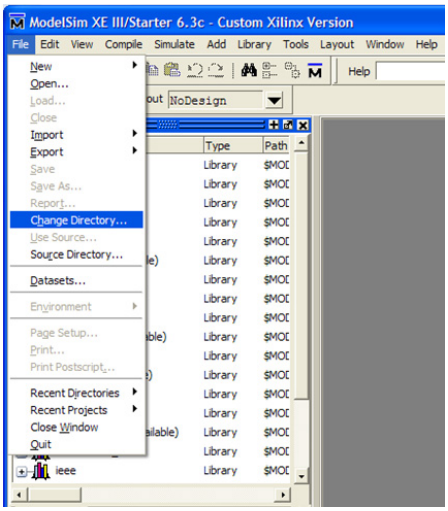
Verilog Simulation Tutorial with ModelSim

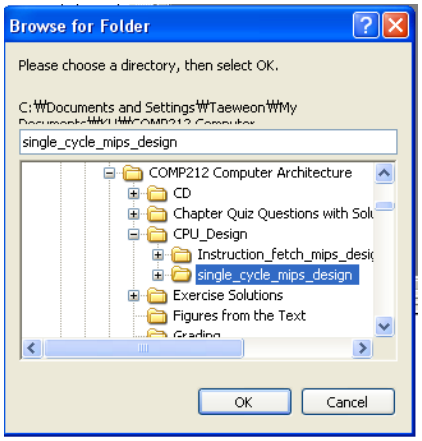
This note summarizes how to do hardware simulation. You are provided with a simple MIPS CPU design in Verilog. The CPU design has implemented only a few MIPS instructions. Its implementation is based on single-cycle execution, meaning that each machine code (instruction) is executed in one clock cycle. The design also comes with a simple testbench. The test assembly program is loaded in the instruction memory after compilation. For hardware simulation, we use a CAD (Computer Aided Design) tool called ModelSim, which is widely used in industry for the hardware simulation. Follow the steps below to run the MIPS CPU design with ModelSim.

1. Download the MIPS CPU design from the class web
   - http://comedu.korea.ac.kr/~suhtw/teaching/comp212_computer_architecture/single_cycle_mips_design.zip

2. Invoke the ModelSim
   - Install ModelSim Altera **Starter** Edition if ModelSim is not installed on your PC
   - http://www.altera.com/products/software/quartus-ii/modelsim/qts-modelsim-index.html

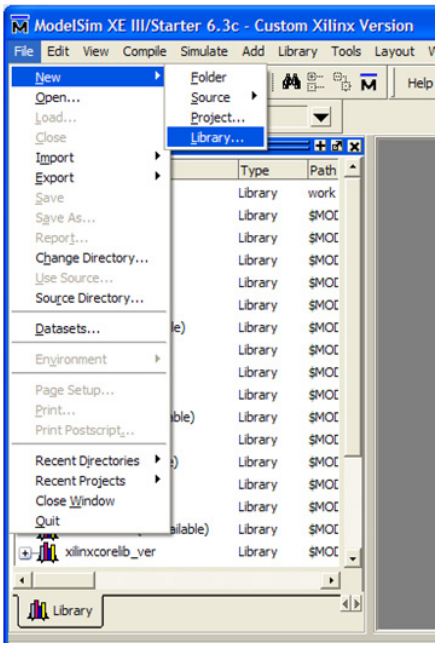
3. Change to the directory where you uncompressed the Verilog sources to
   - "File" → "Change Directory"

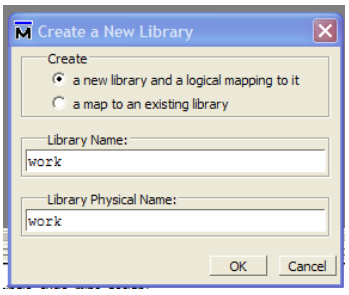




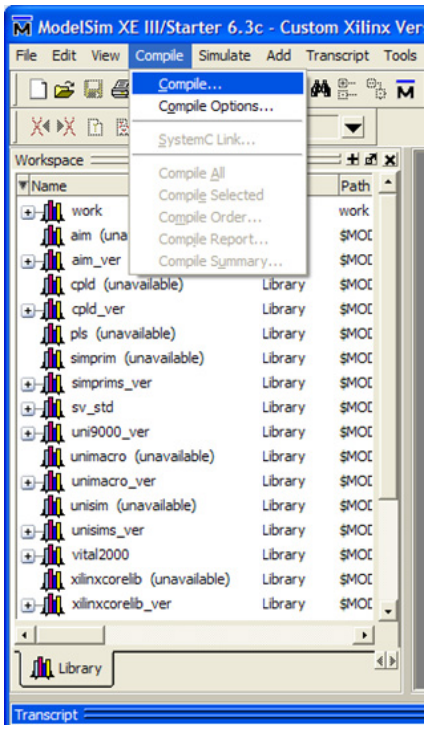
4. Create a library
   - By default, it will show "work" as your library
     - ✓Leave it as it is, and click "OK"
     - ✓Type "work" if it is not set by default
   - You are going to compile the Verilog code with ModelSim
     - ✓During the compilation process, the tool checks if your code conforms to the Verilog syntax

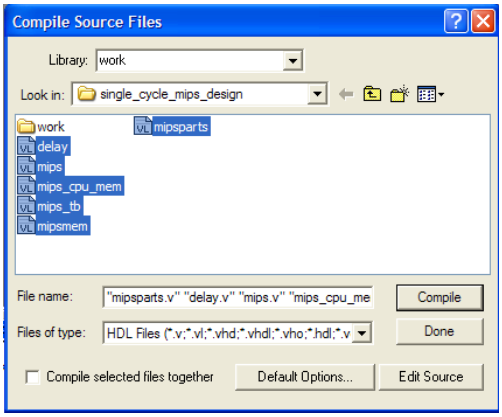
✓The compiled versions of the Verilog sources will be located in the "work" library you just created





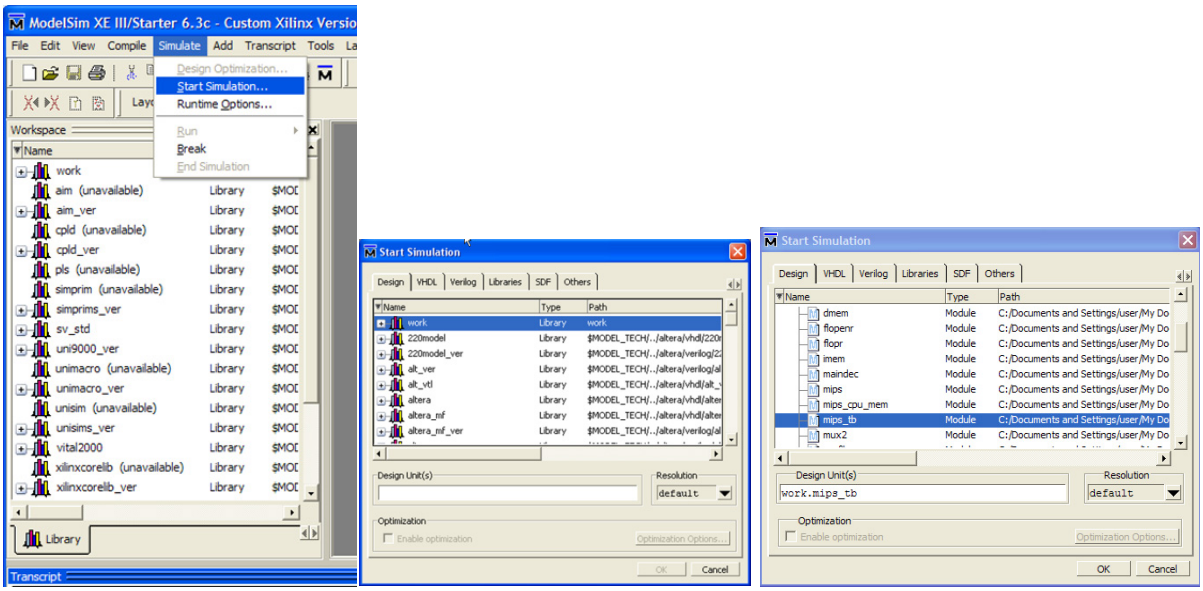
5. Compile the Verilog sources
   - Select all the source files and press "Compile"



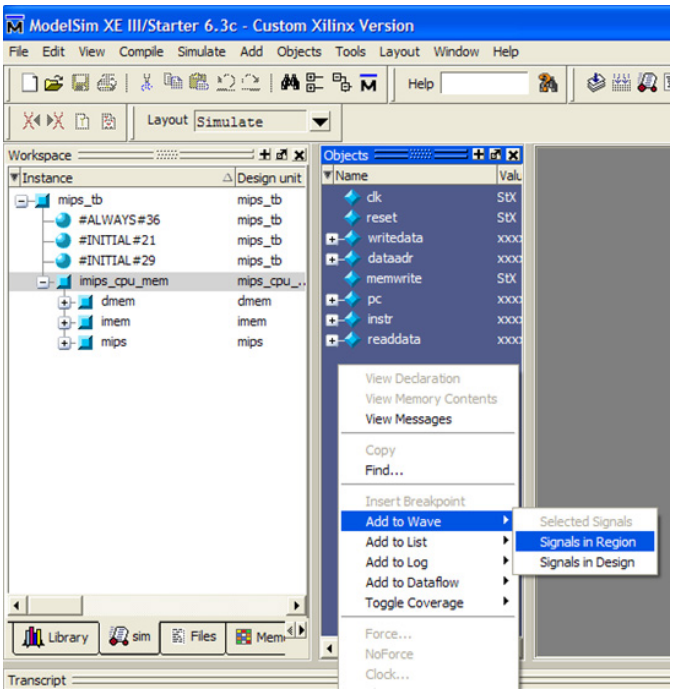


6. Start Simulation
   - "Simulate" → "Start Simulation"

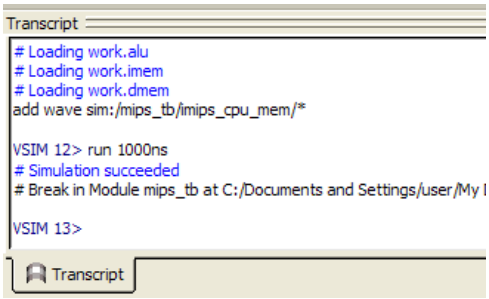
- Select the testbench file “mips_tb” and press “OK”



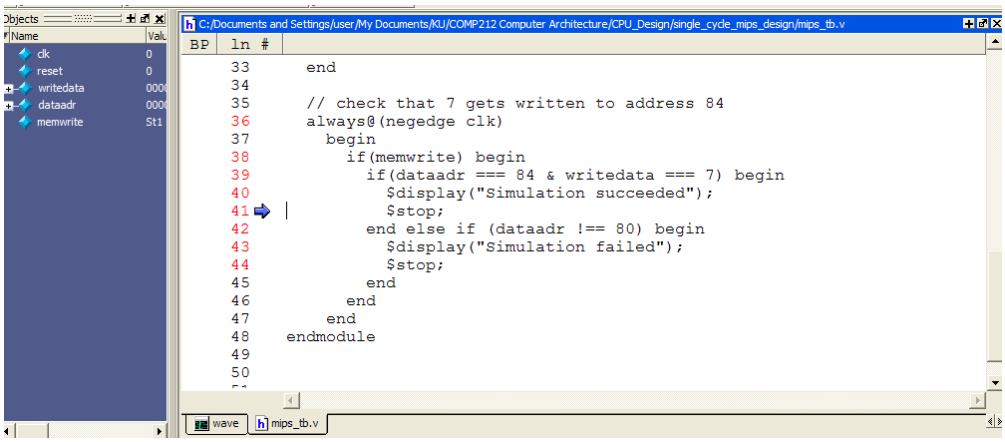
7. Add the signals you want to watch in the waveform
   - Select “imips_cpu_mem”
   - Right-click on the “Objects” pane
     - ✓“Add to wave” → “Signals in Region”



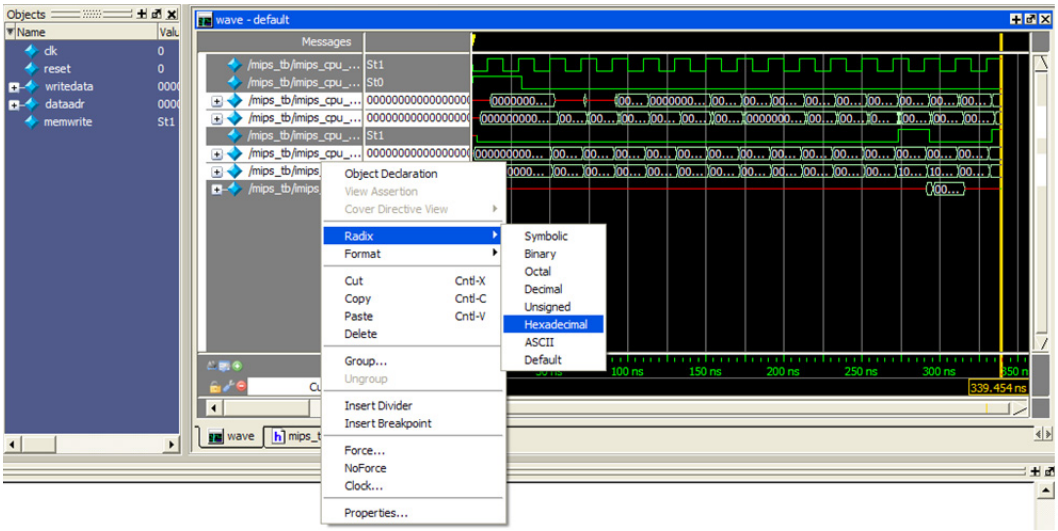
8. Run simulation
   - Type “run 1000ns”
     - ✓It means that the simulation will run for 1000ns

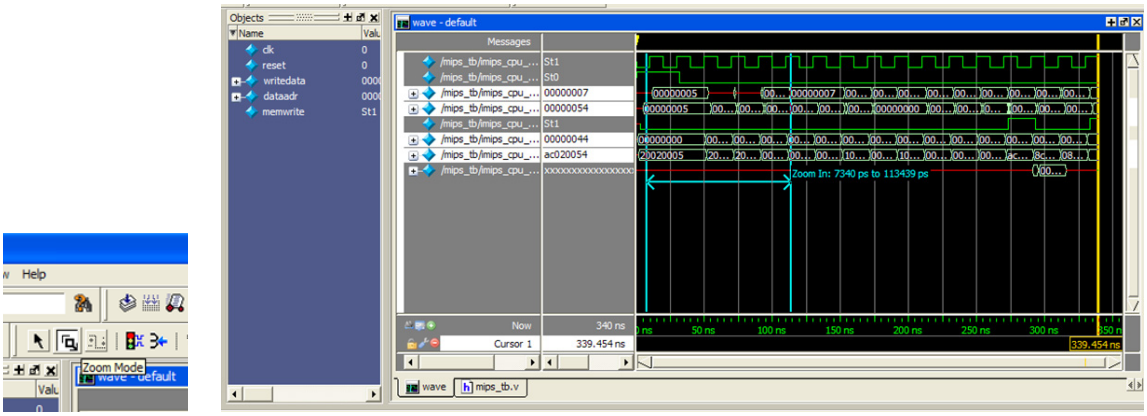


- The simulation should stop with showing the following message
  - ✓Check out the testbench file (mips_tb.v) to see why it stops there



- Click on the "wave" tab and observe the signals (such as PC, fetched instructions, control signals, ALU output etc) you want to watch
  - ✓Change the radix to Hexadecimal for buses
  - ✓Use the zoom mode to zoom in the area you are interested in





9. To restart the simulation
    - Type “restart” and click on “Restart” button
    - Add more signals to the wave if you want to add more signals
        - ✓Go back to step 7 to see how to add signals to the wave
    - Run simulation
        - ✓For example, type “run 100ns” in the transcript pane as you did in the step 8