

2010 R&E: Computer System Education & Research

Simple Timing Analysis with Quartus-II

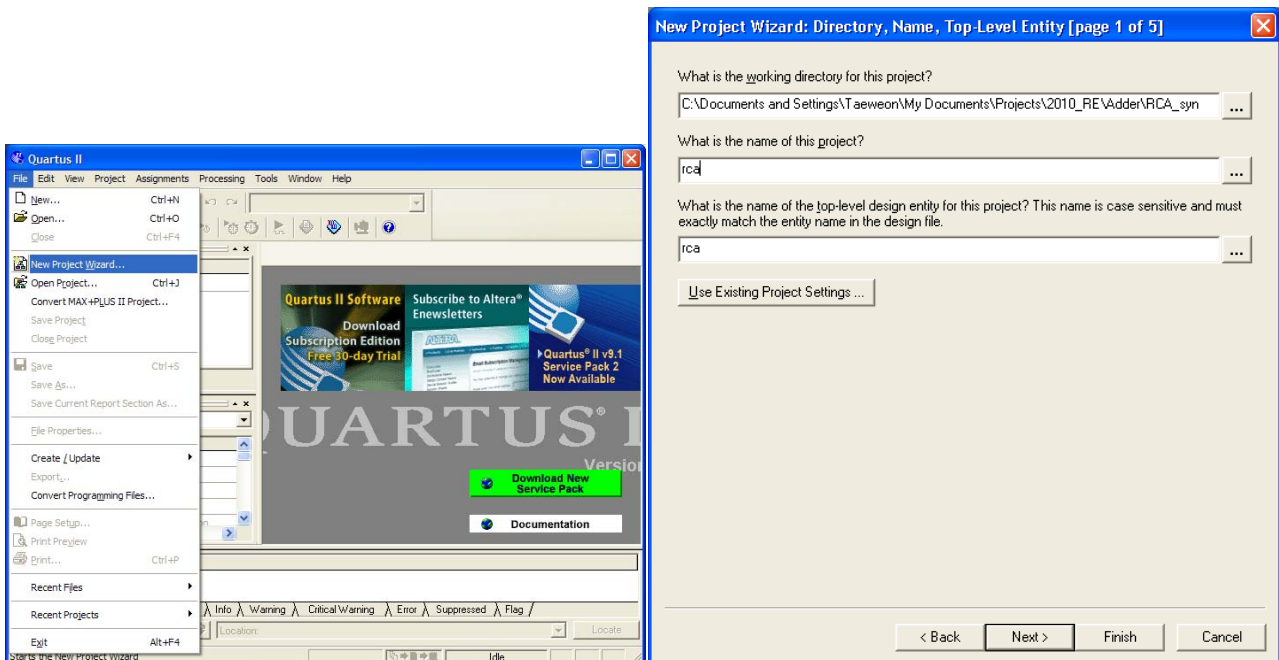
This tutorial will walk you through a simple timing analysis with Quartus-II. With a RCA (Ripple-carry adder) example, you can determine the operating clock frequency of the RCA. First, download the RCA design from the following link.

http://comedu.korea.ac.kr/~suhtw/Research/2010_RE/RCA.zip

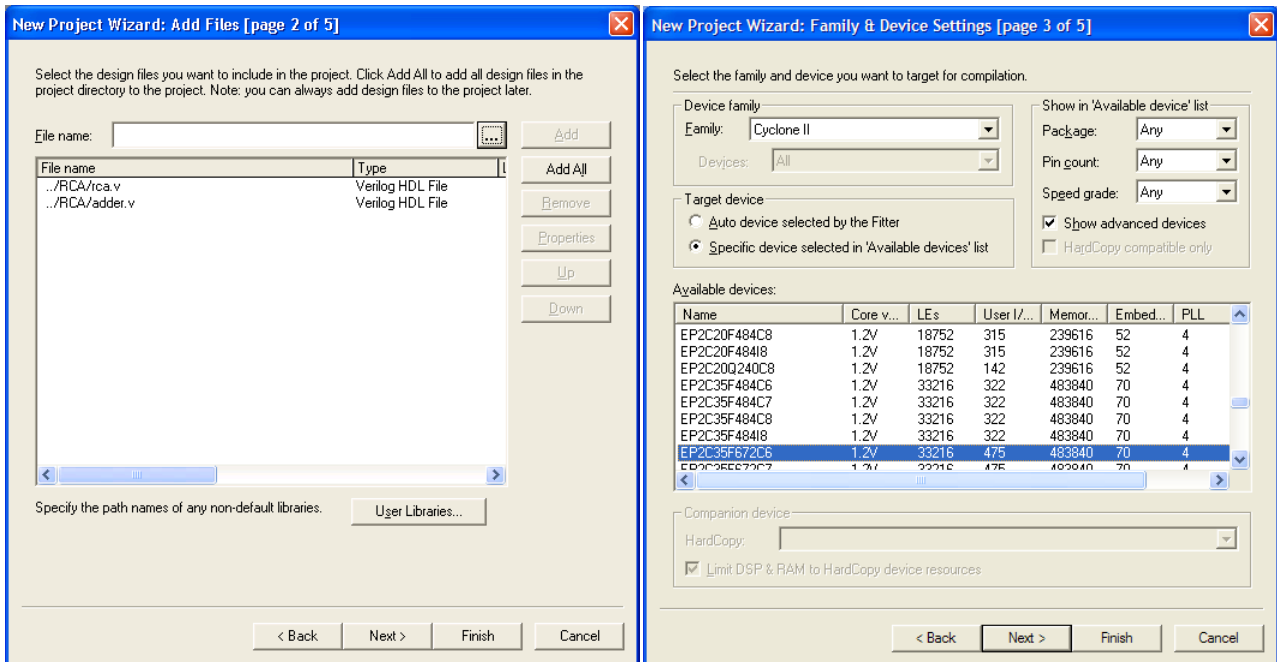
The zip includes an n-bit RCA and a testbench. Open the files and make sure that you understand the operation of the RCA. Next, **run the ModelSim simulation** to check the functionality (you can add testvectors in testbench)

Procedure for Simple Timing Check

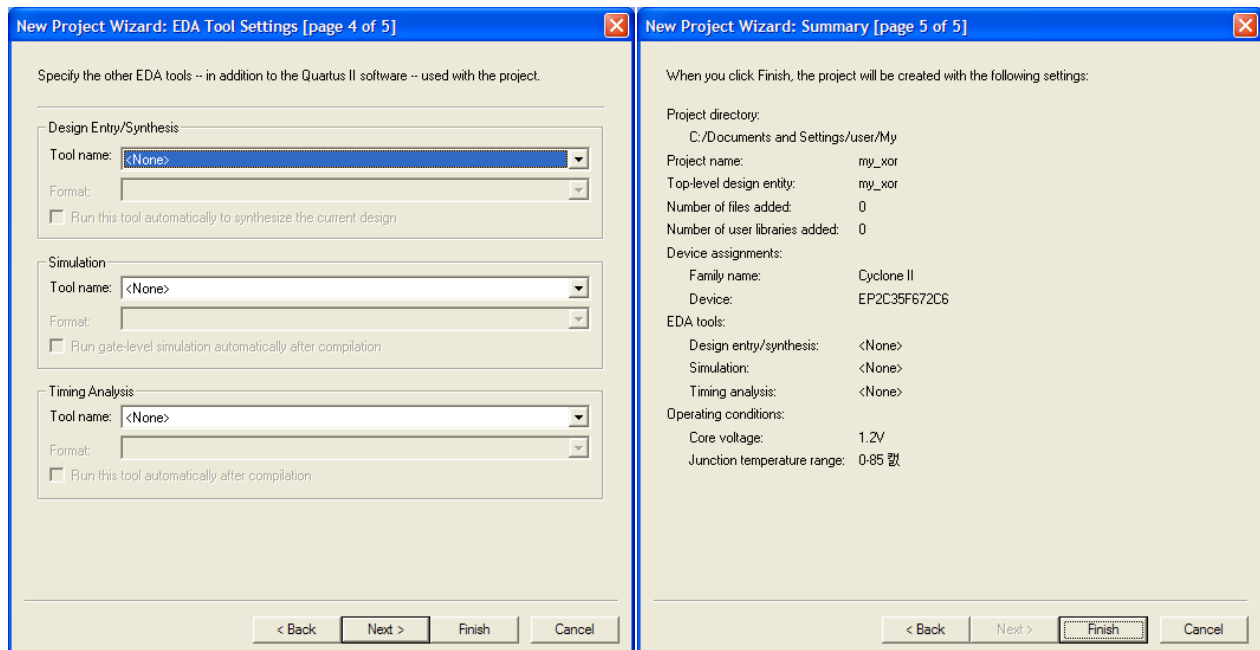
1. Create a new project.
2. Change to a directory where you want to put your project and **make sure that the project name is rca** (it should be the same as the top module name of your design).



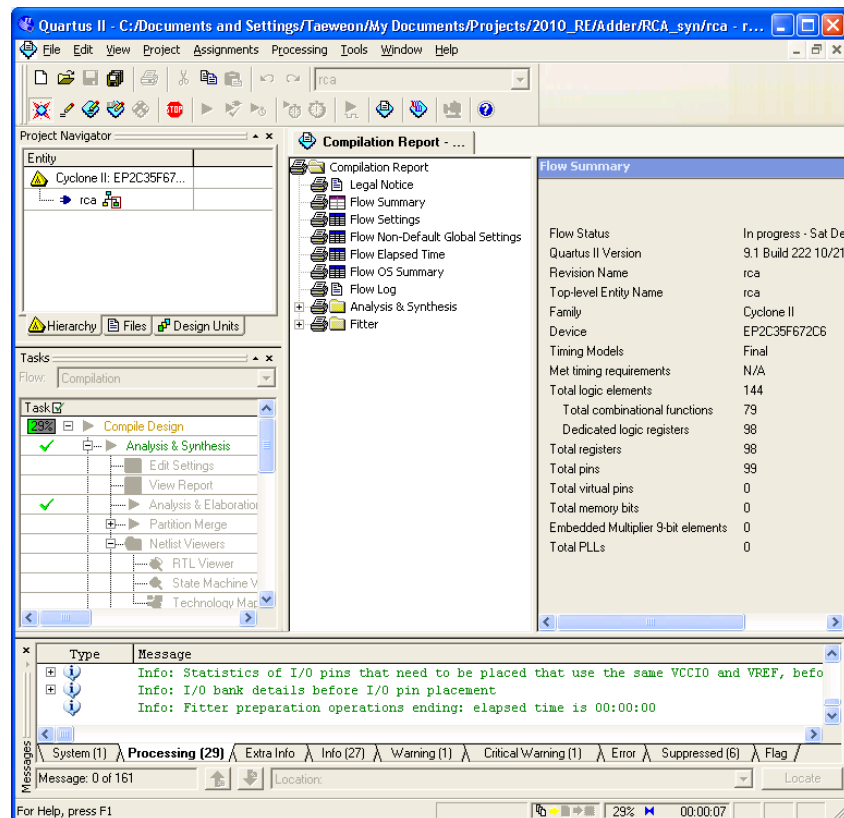
3. Add `rca.v` and `adder.v`, and choose the FPGA device (Cyclone II EP2C35F672C6) as follows



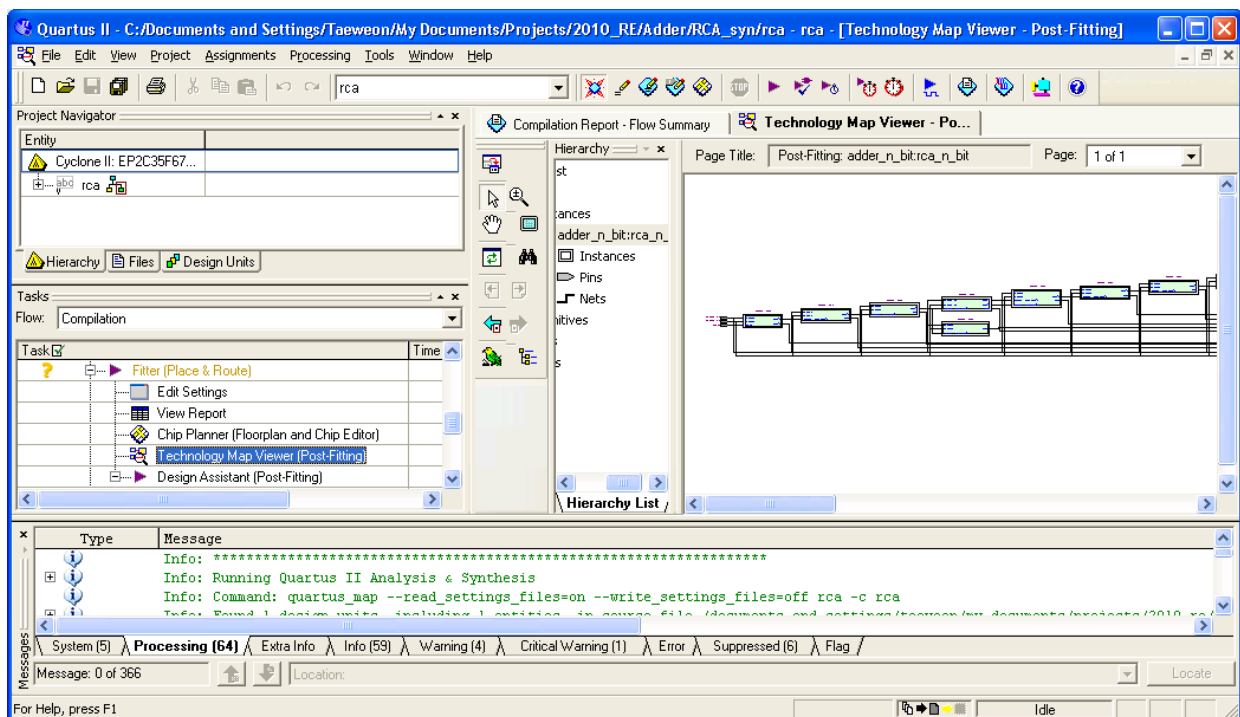
4. Skip the "EDA Tool Settings" and click on "Finish"



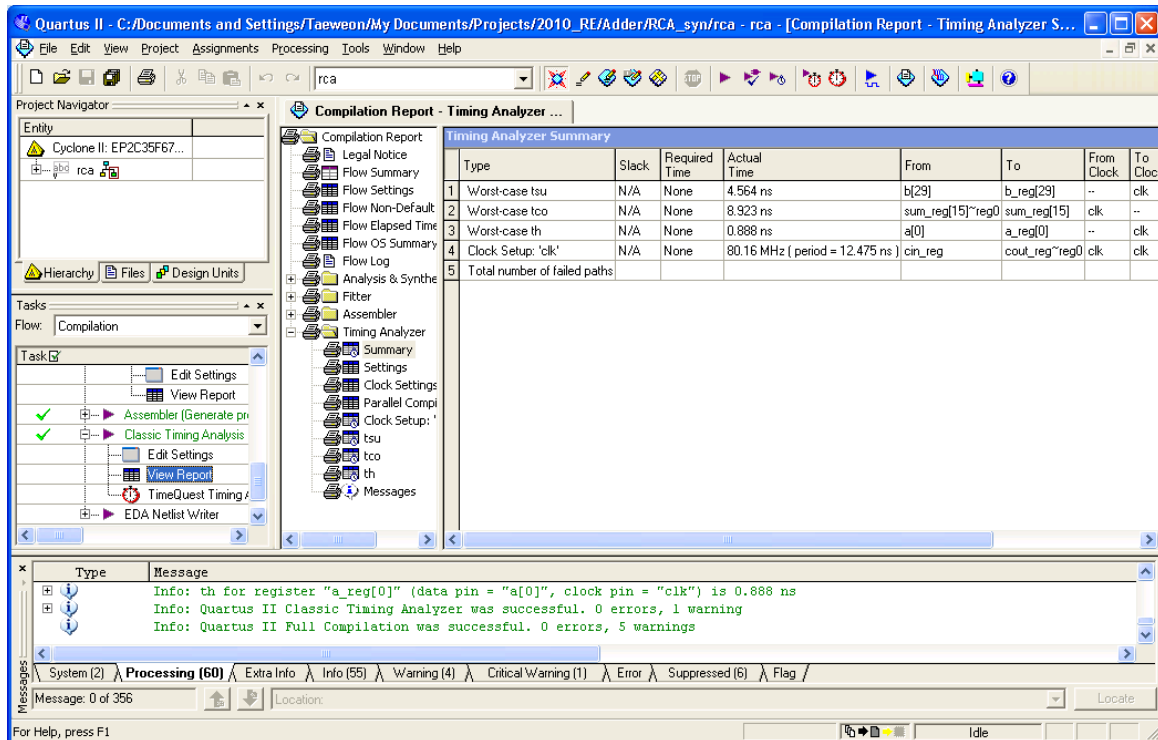
5. The RCA design is configured as 32-bit adder (refer to rca.v). Compile the design to make sure that there is no error.



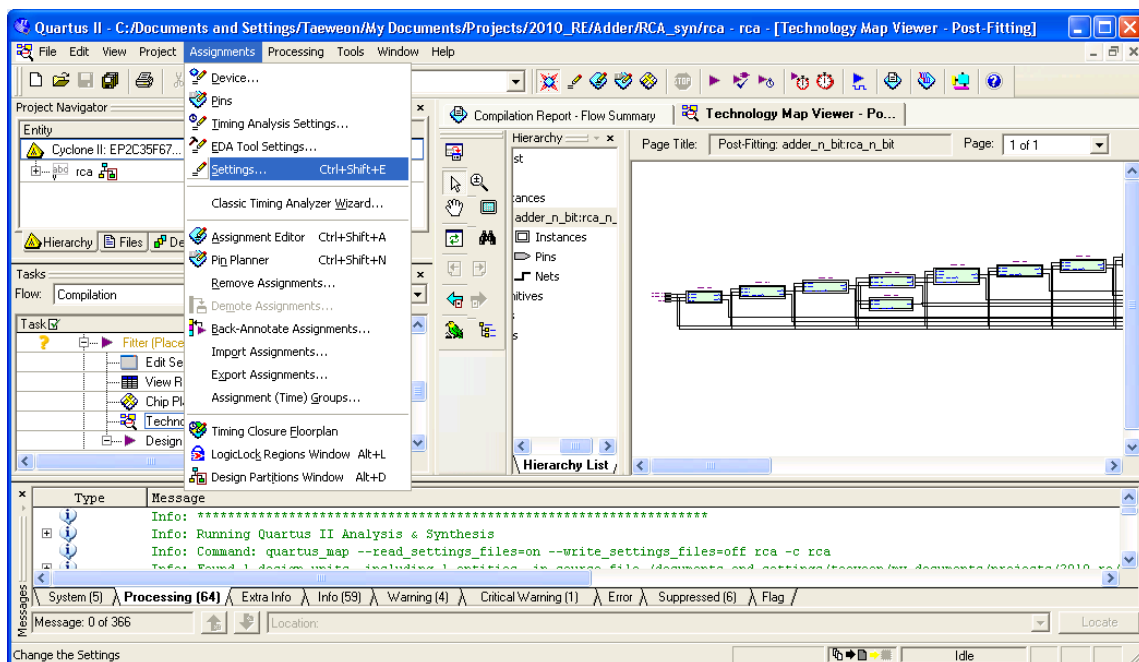
6. Double-click on **Technology Map Viewer (Post-Fitting)** for a schematic view

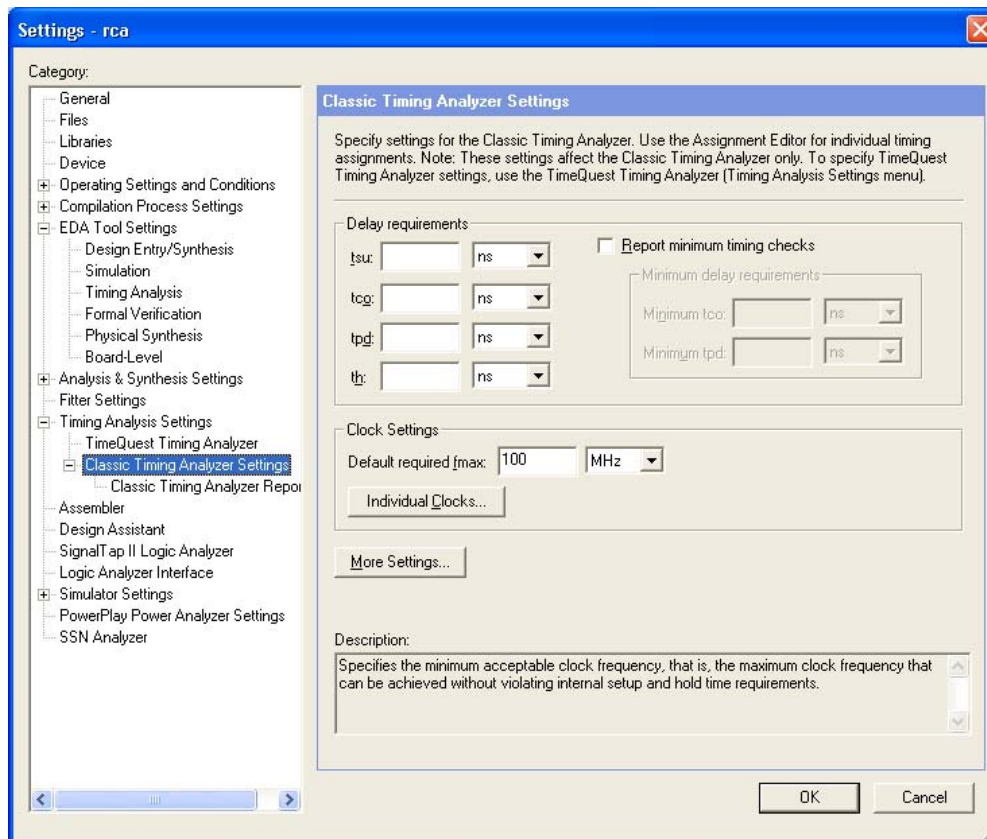


7. Double-click on **View Report** to the clock frequency the design can operate
 - In the example, it is able to run at 80.16MHz (clock period = 12.475ns)



8. You can set a timing constraint (**Assignments** → **Settings**)
 - Set the desired clock frequency in Classic Timing Analyzer Setting
 - ✓ In the example below, we set it to 100MHz
 - ✓ Quartus-II will do its best to meet the constraint (But, it may or may not be able to satisfy the constraint)





- Run **Classic Timing Analysis** again to see if it is able to satisfy the timing constraint
 - It is **NOT** able to run at 100MHz as shown below.
 - 81.55MHz would be the best Quartus-II can do...

Quartus II - C:/Documents and Settings/Taeveon/My Documents/Projects/2010_RE/AddeRCA_syn/rca - rca - [Compilation Report - Timing Analyzer S...

File Edit View Project Assignments Processing Tools Window Help

Project Navigator

- Entity
 - Cyclone II: EP2C35F67...
 - rca
- Hierarchy
 - Files
 - Design Units

Tasks

Flow: Compilation

Task List

- Assembler (Generate programming files)
- Classic Timing Analysis** (00:00)
- Edit Settings
- View Report
- TimeQuest Timing Analyzer
- EDA Netlist Writer

Compilation Report - Timing ...

Timing Analyzer Summary

Type	Slack	Required Time	Actual Time
1 Worst-case tsu	N/A	None	4.544 ns
2 Worst-case tco	N/A	None	7.839 ns
3 Worst-case th	N/A	None	0.698 ns
4 Clock Setup: 'clk'	-2.262 ns	100.00 MHz (period = 10.000 ns)	81.55 MHz (period = 12.2 ns)
5 Clock Hold: 'clk'	0.524 ns	100.00 MHz (period = 10.000 ns)	N/A
6 Total number of failed paths			

Messages

Type Message

- Info: th for register "b_reg[0]" (data pin = "b[0]", clock pin = "clk") is 0.698 ns
- Critical Warning: Timing requirements for slow timing model timing analysis were not met. See Report window for details.**
- Info: Quartus II Classic Timing Analyzer was successful. 0 errors, 4 warnings

System (11) Processing (15) Extra Info Info (11) Warning (3) Critical Warning (1) Error Suppressed Flag

Message: 0 of 176

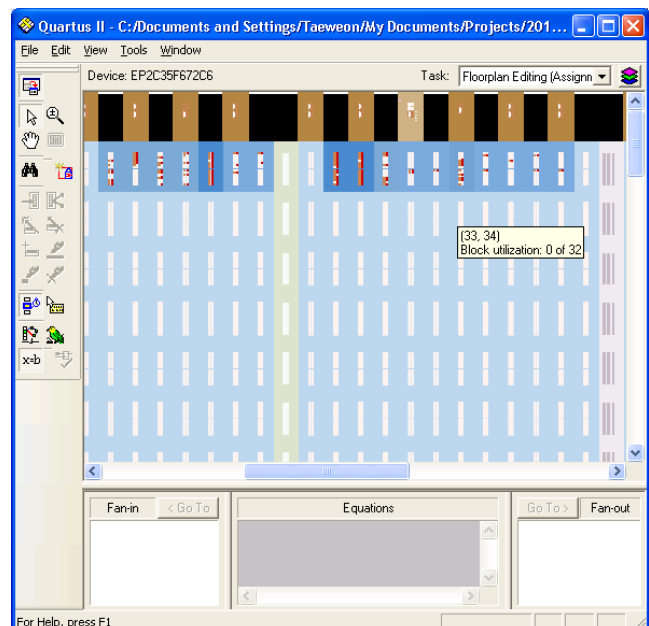
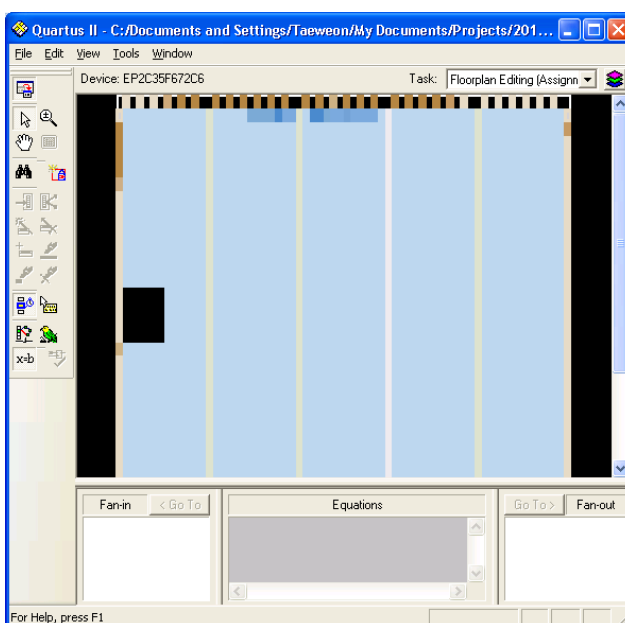
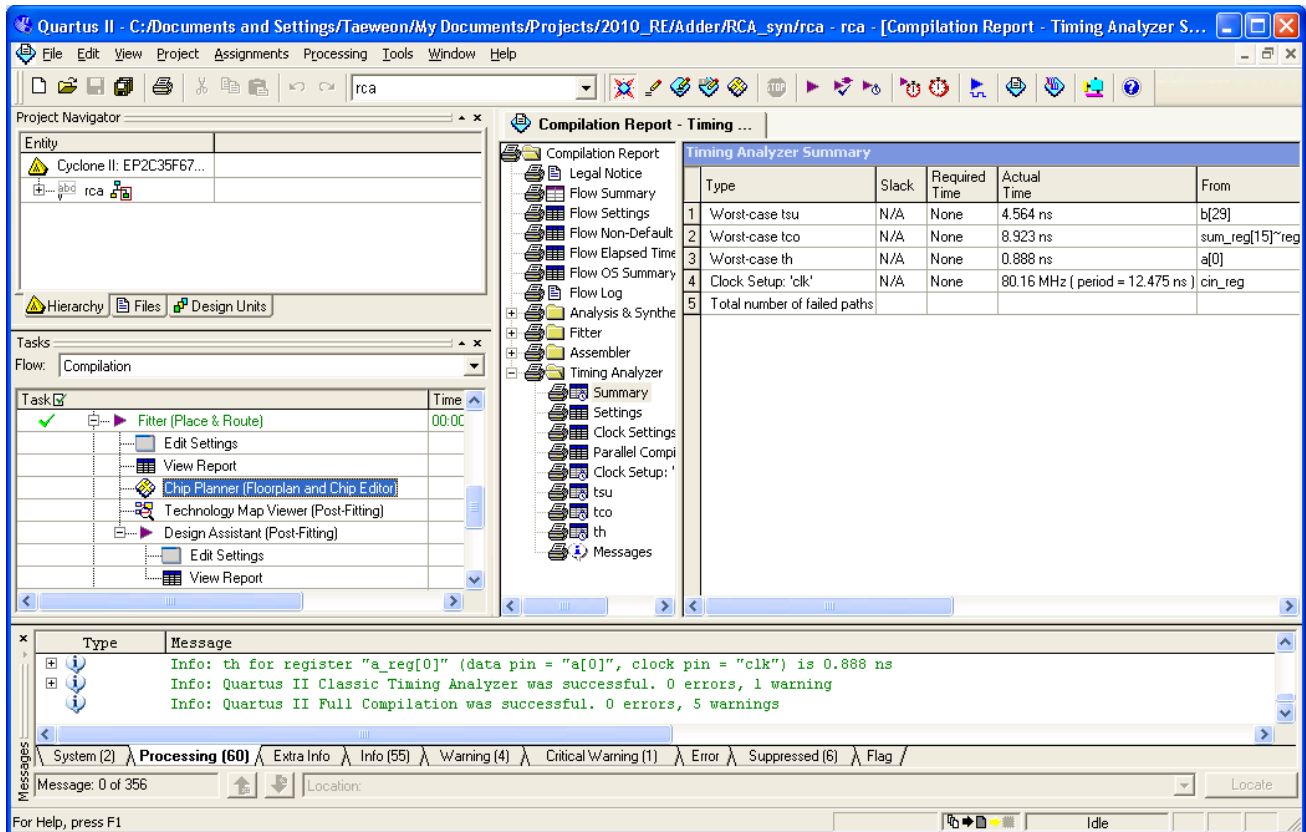
Location: []

For Help, press F1

Idle

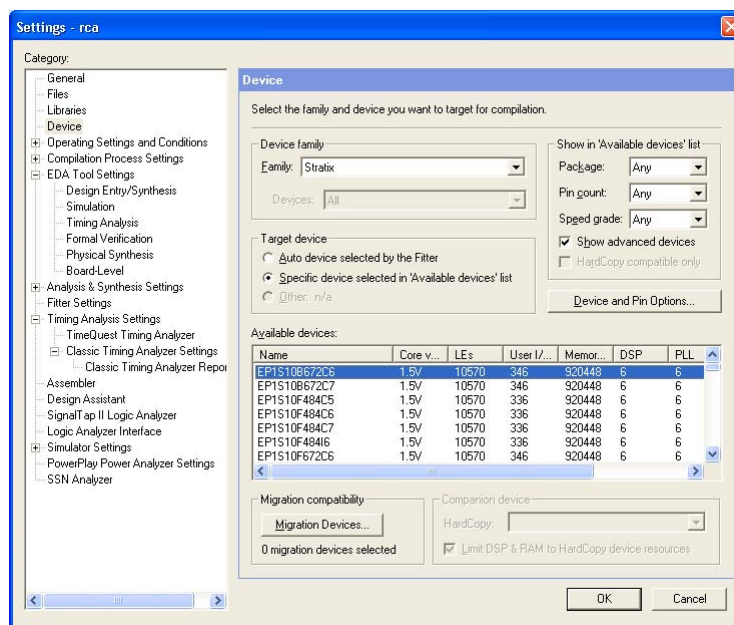
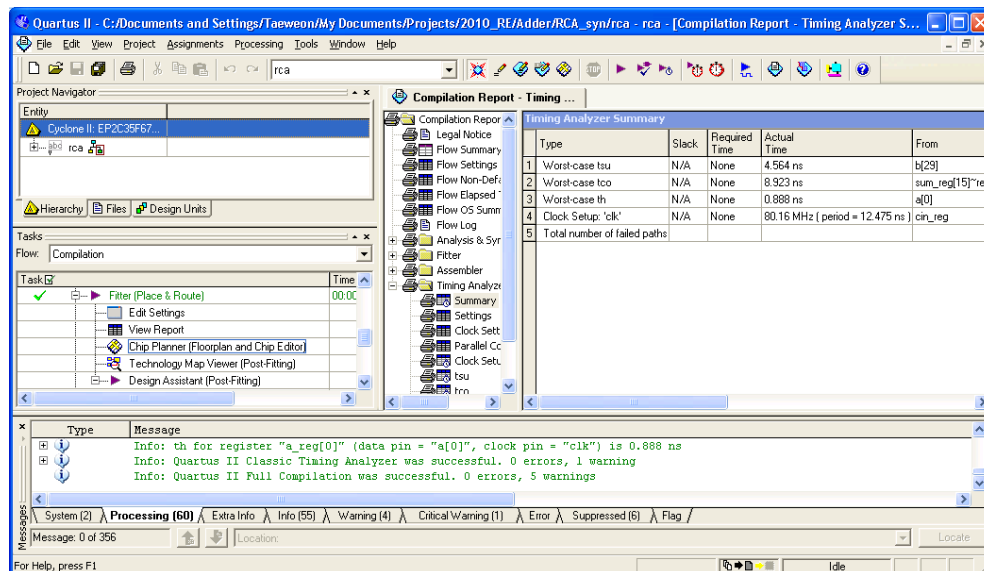
10. To view how much FPGA space is allocated for the adder, double-click on **Chip Planner (Floorplan and Chip Editor)**.

- Then, a new window will pop up as shown below
- Rectangles in cyan and blue are the space allocated for the adder. If you want to zoom in, stay pressing **ctrl** and roll up the mouse wheel



Next Steps

- Change the RCA from 8-bit, 16-bit, 32-bit, 64-bit, 128-bit and 256-bit. For each adder, measure the operating clock frequency
 - You can draw a graph based on the data collected
 - ✓ x-axis is the width of adders (8-bit, 16-bit ...)
 - ✓ y-axis is the delay (12.475ns in the example) (or frequency)
- Change the FPGA device and do the same experiment as in step 1
 - For example, from **Cyclone II** to **Stratix (and Cyclone-III, Cyclone-IV, Stratix-II, Stratix-III, Arria GX, and Arria II GX)**
 - Double-click on **Cyclone II EP2C35F672C6** and a new window will pop up as shown below
 - So, you can draw a graph for each device



3. Repeat the step 1 and step 2 for **prefix adder** you have designed
4. You can **compare the performance (clock frequency) of RCA and prefix adder in FPGA** by putting together it in one graph
 - In the paper, you may want to include the notable schematic and chip floorplan views as well.
5. If possible, perform the same experiment with **Xilinx** FPGAs
 - You need to download a new tool (ISE) from the web (www.xilinx.com) for it!