2010 R&E: Computer System Education & Research

Simple Timing Analysis with Quartus-II

This tutorial will walk you through a simple timing analysis with Quartus-II. With a RCA (Ripple-carry adder) example, you can determine the operating clock frequency of the RCA. First, download the RCA design from the following link.

http://comedu.korea.ac.kr/~suhtw/Research/2010_RE/RCA.zip

The zip includes an n-bit RCA and a testbench. Open the files and make sure that you understand the operation of the RCA. Next, **run the ModelSim simulation** to check the functionality (you can add testvectors in testbench)

Procedure for Simple Timing Check

- 1. Create a new project.
- 2. Change to a directory where you want to put your project and make sure that the project name is rca (it should be the same as the top module name of your design).

	New Project Wizard: Directory, Name, Top-Level Entity [page 1 of 5]
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3. Add rca.v and adder.v, and choose the FPGA device (Cyclone II EP2C35F672C6) as follows

New Project Wizard: Add Files [page 2 of 5]	New Project Wizard: Family & Device Settings [page 3 of 5]
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4. Skip the "EDA Tool Settings" and click on "Finish"

New Project Wizard: EDA Tool Settings [page 4 of 5]	New Project Wizard: Summary [page 5 of 5]	gs:
Specify the other EDA tools in addition to the Quartus II software used with the project.	When you click Finish, the project will be created with the following settings: Project directory:	
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5. The RCA design is configured as 32-bit adder (refer to rca.v). Compile the design to make sure that there is no error.



6. Double-click on Technology Map Viewer (Post-Fitting) for a schematic view



- 7. Double-click on **View Report** to the clock frequency the design can operate
 - In the example, it is able to run at 80.16MHz (clock period = 12.475ns)

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- 8. You can set a timing constraint (Assignments → Settings)
 - Set the desired clock frequency in Classic Timing Analyzer Setting
 - \checkmark In the example below, we set it to 100MHz
 - ✓Quartus-II will do its best to meet the constraint (But, it may or may not be able to satisfy the constraint)



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Settings - rca Category: General Files Libraries Device Operating Settings and Conditions Compilation Process Settings EDA Tool Settings Design Entry/Synthesis Simulation Timing Analysis Formal Venification Physical Synthesis Board-Level Analysis & Synthesis Settings Fitter Settings Timing Analysis Settings	Classic Timing Analyzer Settings Specify settings for the Classic Timing Analyzer. Use the Assignment Editor for individual timing assignments. Note: These settings affect the Classic Timing Analyzer only. To specify TimeQuest Timing Analyzer settings, use the TimeQuest Timing Analyzer (Timing Analyzer Settings menu). Delay requirements tsu: tog: ns: tg: ns: Clock Settings
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- 9. Run Classic Timing Analysis again to see if it is able to satisfy the timing constraint
 - It is **NOT** able to run at 100MHz as shown below.
 - 81.55MHz would be the best Quartus-II can do...

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- 10. To view how much FPGA space is allocated for the adder, double-click on **Chip Planner** (Floorplan and Chip Editor).
 - Then, a new window will pop up as shown below
 - Rectangles in cyan and blue are the space allocated for the adder. If you want to zoom in, stay pressing **ctrl** and roll up the mouse wheel

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Next Steps

- 1. Change the RCA from 8-bit, 16-bit, 32-bit, 64-bit, 128-bit and 256-bit. For each adder, measure the operating clock frequency
 - You can draw a graph based on the data collected
 - \checkmark x-axis is the width of adders (8-bit, 16-bit ...)
 - \checkmark y-axis is the delay (12.475ns in the example) (or frequency)
- 2. Change the FPGA device and do the same experiment as in step 1
 - For example, from Cyclone II to Stratix (and Cyclone-III, Cyclone-IV, Stratix-II, Stratix-III, Arria GX, and Arria II GX)
 - Double-click on Cyclone II EP2C35F672C6 and a new window will pop up as shown below
 - So, you can draw a graph for each device

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- 3. Repeat the step 1 and step 2 for **prefix adder** you have designed
- 4. You can compare the performance (clock frequency) of RCA and prefix adder **in FPGA** by putting together it in one graph
 - In the paper, you may want to include the notable schematic and chip floorplan views as well.
- 5. If possible, perform the same experiment with **Xilinx** FPGAs
 - You need to download a new tool (ISE) from the web (<u>www.xilinx.com</u>) for it!