## 2010 R&E: Computer System Education & Research

## Lab 4. Hardware Synthesis & Simulation

- Download an example Verilog code (sillyfuction.v) with testbench (testbench1.v) from <u>http://comedu.korea.ac.kr/~suhtw/teaching/comp211\_CLD/HW4\_Verilog.zip</u>
- Synthesis
  - Install Altera Quartus-II Web Edition from <u>http://www.altera.com/products/software/quartus-ii/web-</u> <u>edition/qts-we-index.html</u>
  - Follow the synthesis steps from page 2
  - Screen-capture the synthesized logic
- Simulation
  - Install Altera ModelSim Starter Edition on your PC from <u>http://www.altera.com/products/software/quartus-ii/modelsim/qts-modelsim-index.html</u>
  - Follow the simulation steps from page 6
  - Screen-capture the waveform, showing the meaningful section.

## • Synthesis Steps

- Invoke the Quartus-II
   Create a new project

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Starts the New Project Wizard	

3. Go to any directory where you want to create your project and type a project name of your choice

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What is the name of this project?	
sillyfunction	
What is the name of the top-level design exactly match the entity name in the design exactly e	gn entity for this project? This name is case sensitive and must esign file.
sillyfunction	
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4. Choose 'Cyclone-II' in Device Family and 'EP2C35F672C6' among available devices (The device is on DE 2 Board shown in the class)

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5. Then 'Next  $\rightarrow$  Next  $\rightarrow$  Finish'



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- 6. Then 'Project  $\rightarrow$  Add/Remove Files' in Project

7. Click on `...' besides File name, add `sillyfunction.v' from the download and then click `Add' button.





8. Double-click on 'RTL Viewer' to generate schematic



## • Simulation Steps

1. Invoke the ModelSim Altera Edition, 'File  $\rightarrow$  Change Directory' and choose a directory where simulation files are going to be saved

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2. 'File  $\rightarrow$  New  $\rightarrow$  Library' and you can type a library name of your choice, but let's leave the name (work) as it is

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3. Compile the Verilog code you have downloaded by `Compile  $\rightarrow$  Compile' and choose both sillyfunction.v and testbench1.v

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4. Run simulation by `Simulation  $\rightarrow$  Start Simulation' and choose testbench1 under work library. Then press OK

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5. Choose 'dut' and add all signals (a, b, c, and y) to the waveform by 'Add  $\rightarrow$  To Wave  $\rightarrow$  Signals in Region"





6. Run simulation for 100ns by typing "run 100ns" in the Transcript pane.

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7. See the full screen of the waveform by 'View → Zoom → Zoom Full'. Is the output (y) shown as you expected?

