2010 R&E: Computer System Education & Research

Lab 3. Combinational Logic Design with Verilog-HDL

Implement the following combinational logic using **Verilog-HDL**.

7 Segment Display

Take a 4-bit input from SW3, SW2, SW1, and SW0 on DE2 board. Since you are taking inputs from 4 switches, it can represent numbers from 0x0 to 0xF. In this lab, let's finish and design the combinational logic discussed in the lecture slides, which can display a decimal number (from 0 to 9) based on the switch inputs.

Priority Encoder

A priority encoder has 2^N inputs. It produces an N-bit binary output, indicating the most significant bit of the input that is TRUE. Design an 8-input priority-encoder with inputs $A_{7:0}$ and outputs $Y_{2:0}$. For example, if the input is 0010_0000, the output Y should be 101 since the bit 5 of the input is 1. Use the 7 segment display logic you designed in the first part to display the number.

Adder & Subtractor

Design a 4-bit adder & subtractor. Since it is a 4-bit adder/subtractor, it takes two 4-bit inputs. Let's take inputs from switches. Use the following guideline to design the adder/subtractor.

- Input 1 is from switch 0 ~ 3 (It can represent numbers from 0 to 15)
- Input 2 is from switch 14 ~ 17 (It can represent numbers from 0 to 15)
- Switch 8 controls the operation (addition if SW8 is down and subtraction if SW8 is up)
- HEX0 (7 segment) displays the operation outcome
- LEDG0 (LED Green 0) displays the carry-out