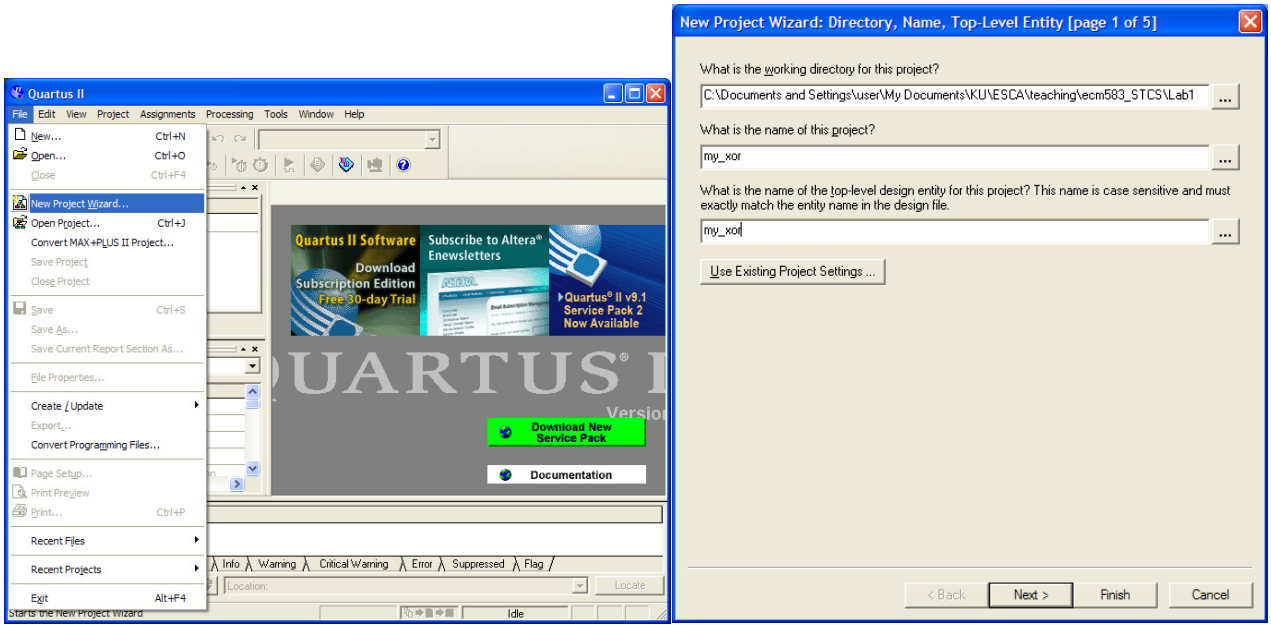
2010 R&E: Computer System Education & Research

Lab 1. Getting Started with DE2 and Quartus-II

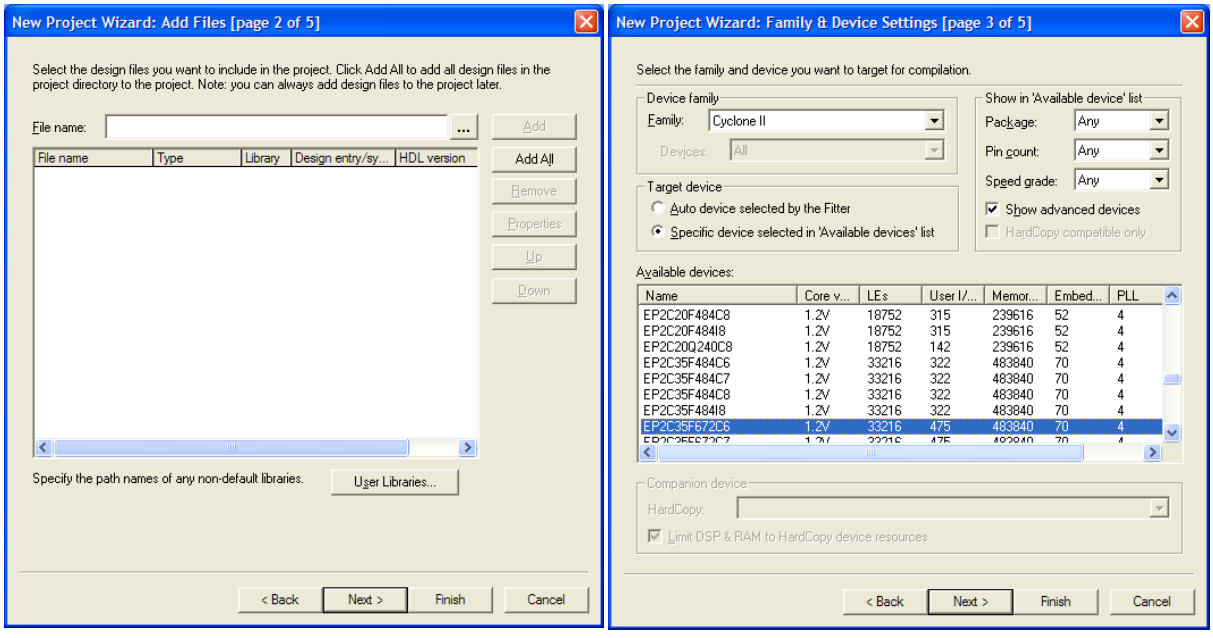
In this lab, we are going to design a simple XOR gate with Quartus-II and download it to DE2 board. There are 2 ways to design the XOR gate: Schematic-based design and HDL-based design. The XOR gate will take inputs from KEY0 and KEY1 in DE2 board and display the output LEDR0 (red LED 0)

1. Schematic-based design

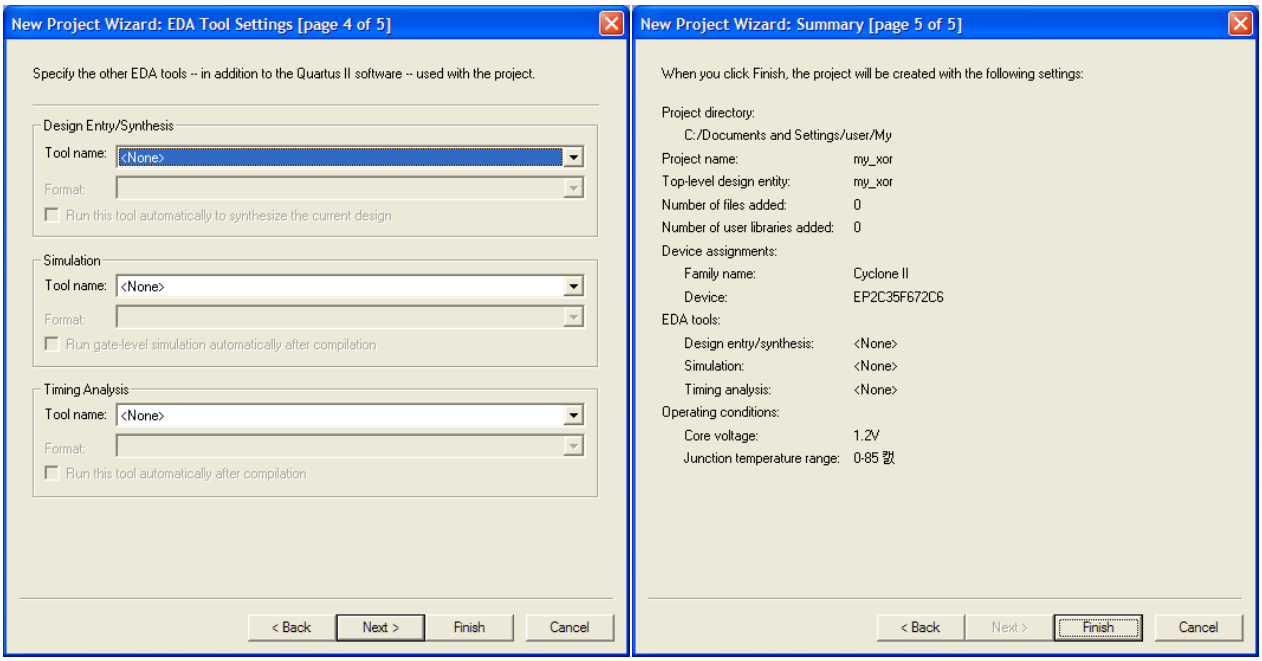
1. Create a new project.
2. Change to the directory where you want to put your project and put your project name of your choice.



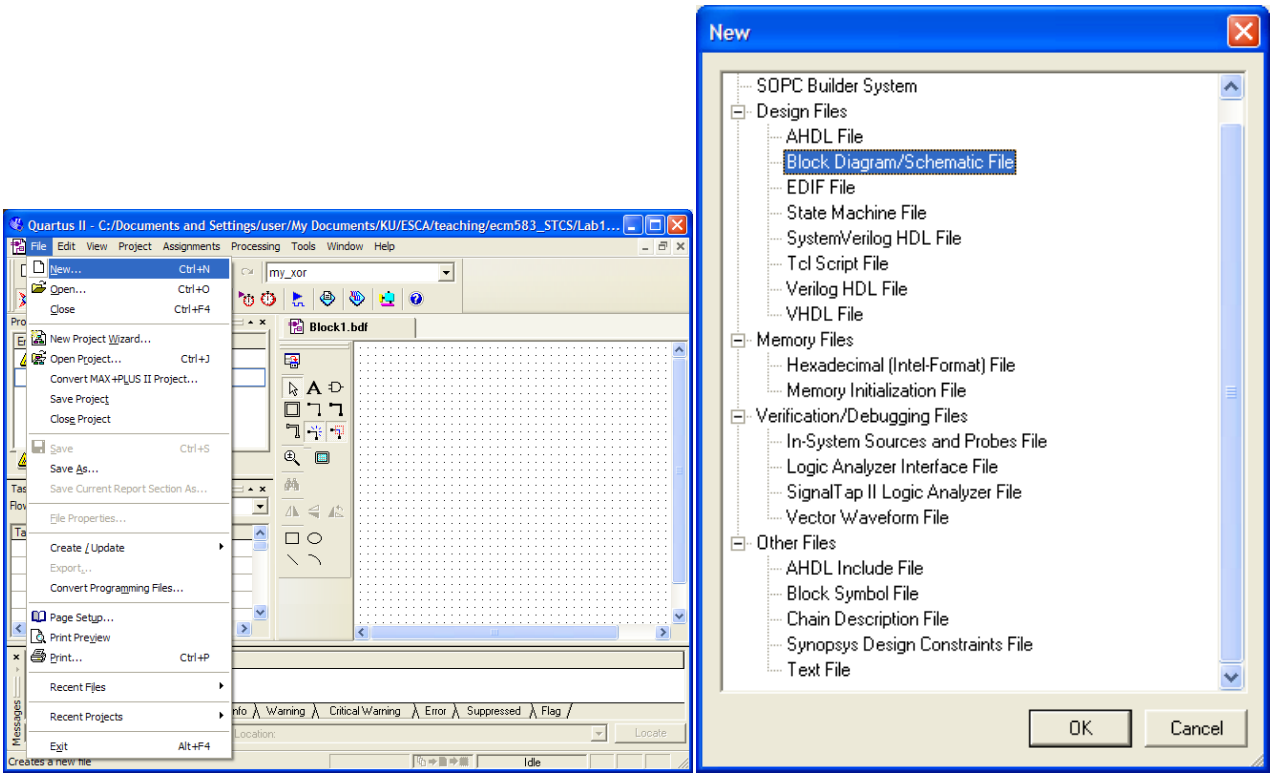
3. Skip the "Add Files" and choose the FPGA device (Cyclone II EP2C35F672C6) as follows



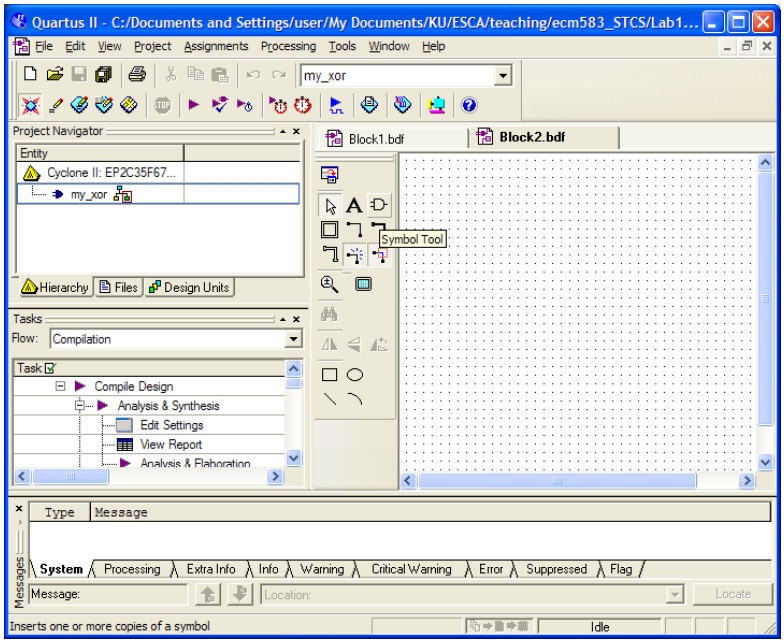
4. Skip the “EDA Tool Settings” and click on “Finish”

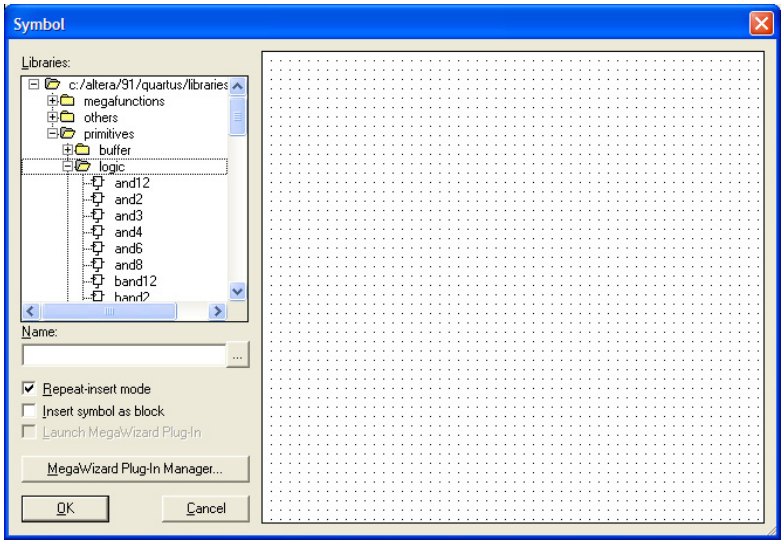


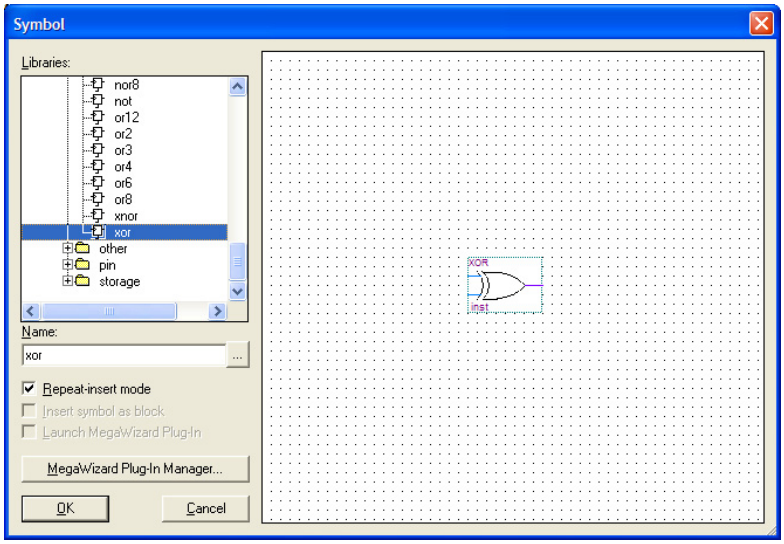
5. File → New
6. Choose “Block Diagram/Schematic File”



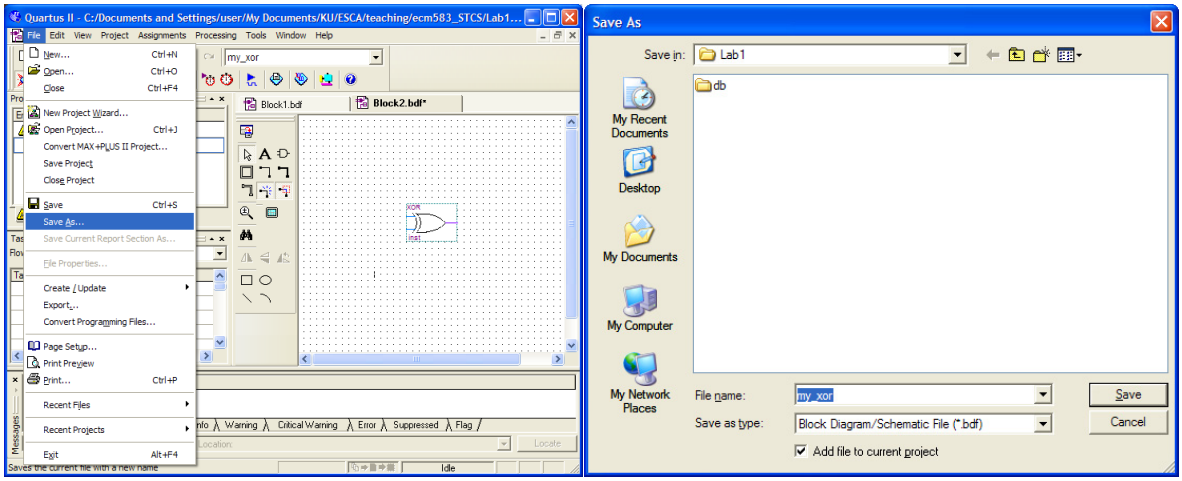
7. Click on “Symbol Tool”, expand by clicking “+”, and select “xor”



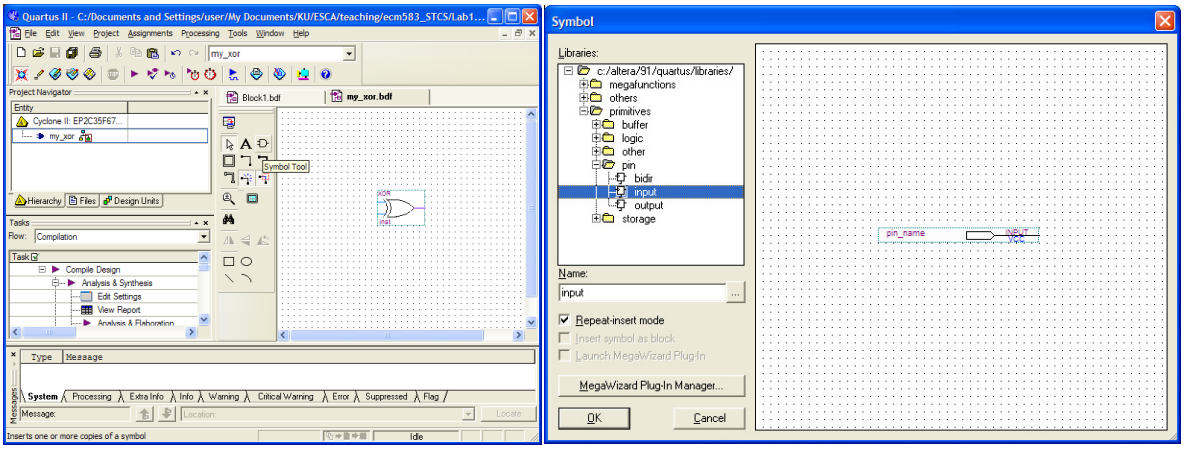




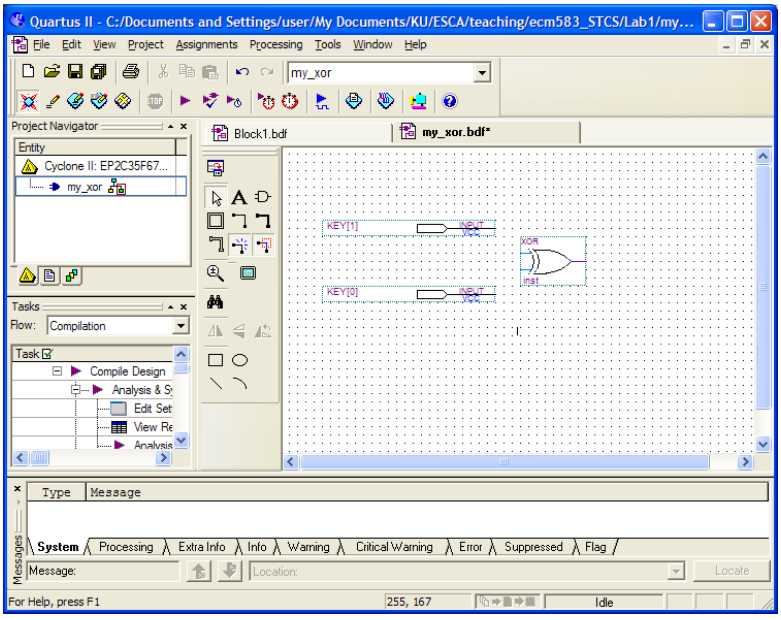
8. “File” → “Save As”, put “my_xor” in the File name, and click on “Save”



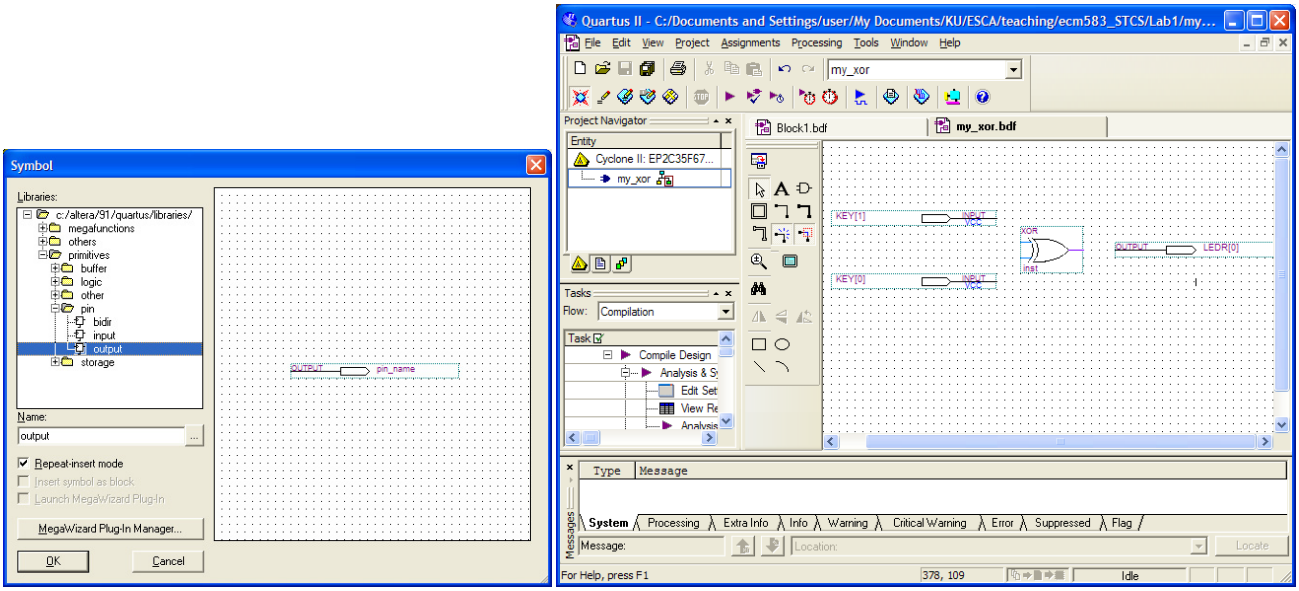
9. Click on “Symbol Tool” and select “input”



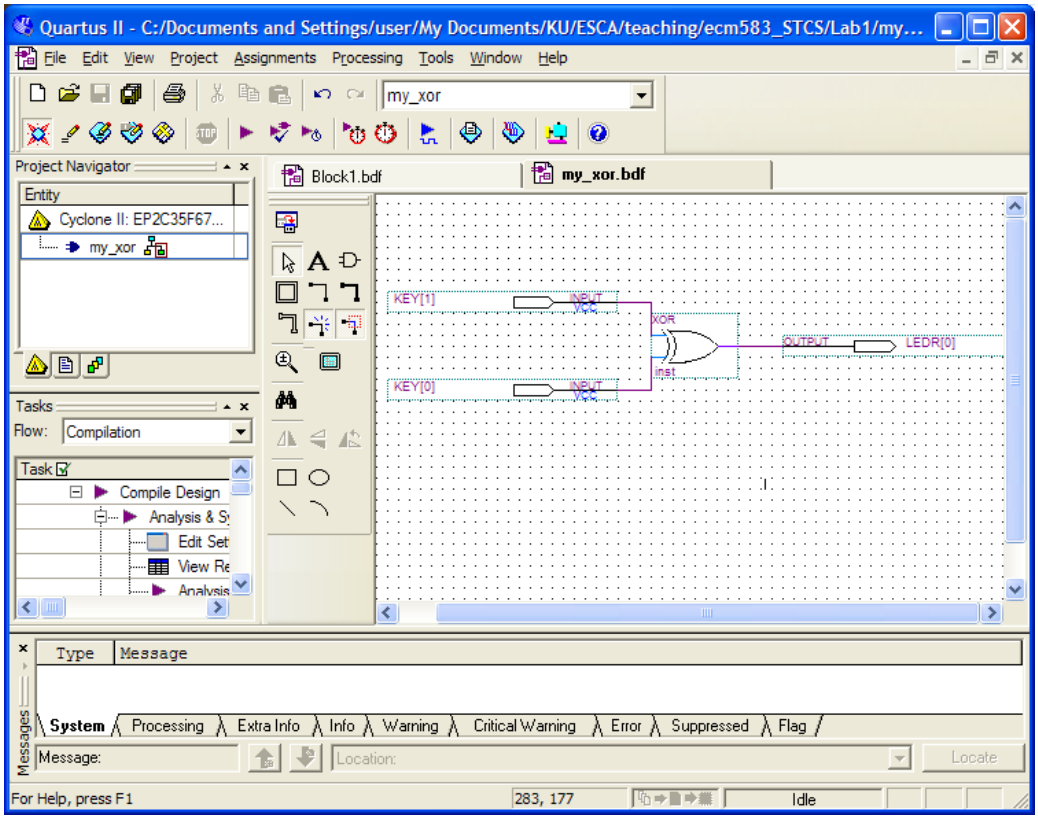
10. Instantiate the input pin two times and name it to “KEY[1]” and “KEY[0]”
    - Note that KEY[1] and KEY[0] are the names that the DE2 board uses to connect to push button keys. Thus, if you use the same names, you don’t have to separately assign it to the FPGA pins later on.



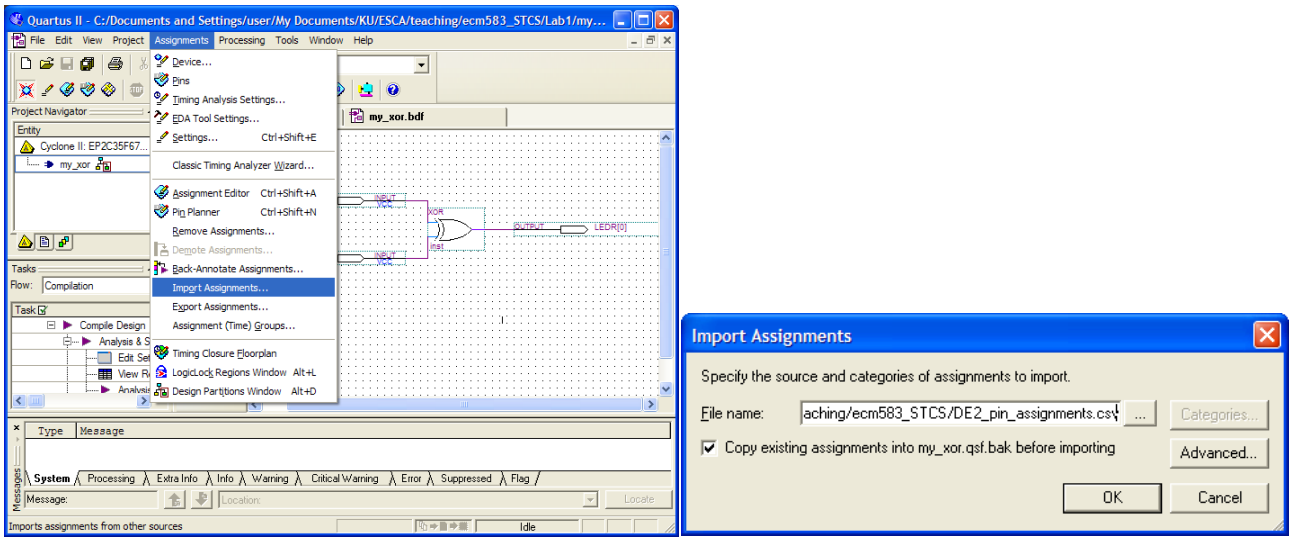
11. Instantiate the output pin and name it to “LEDR[0]”



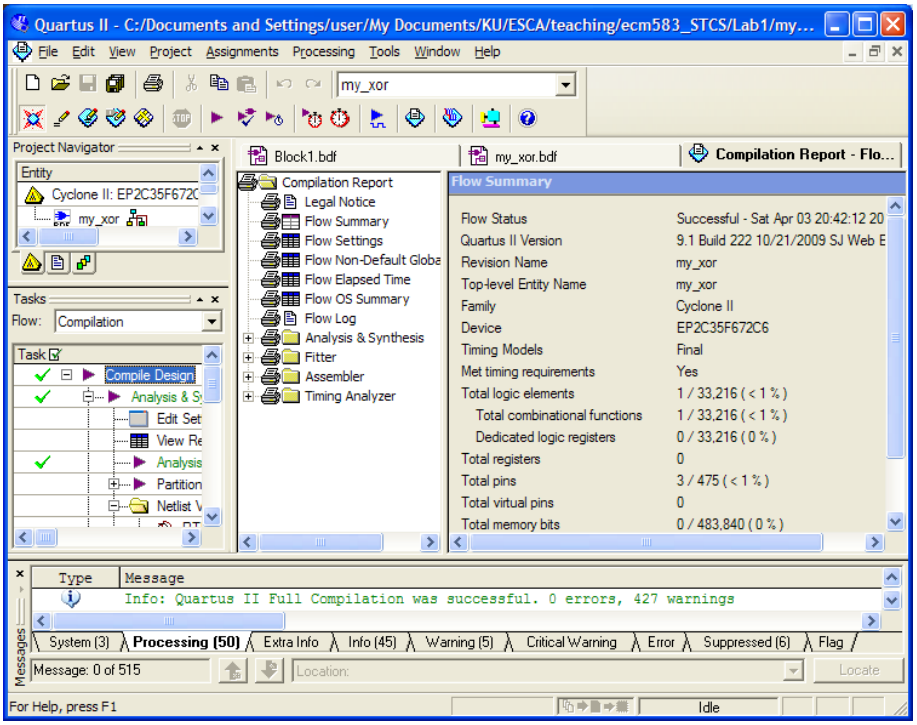
12. Connect the input pins to the xor gate inputs and the xor output to the output pin



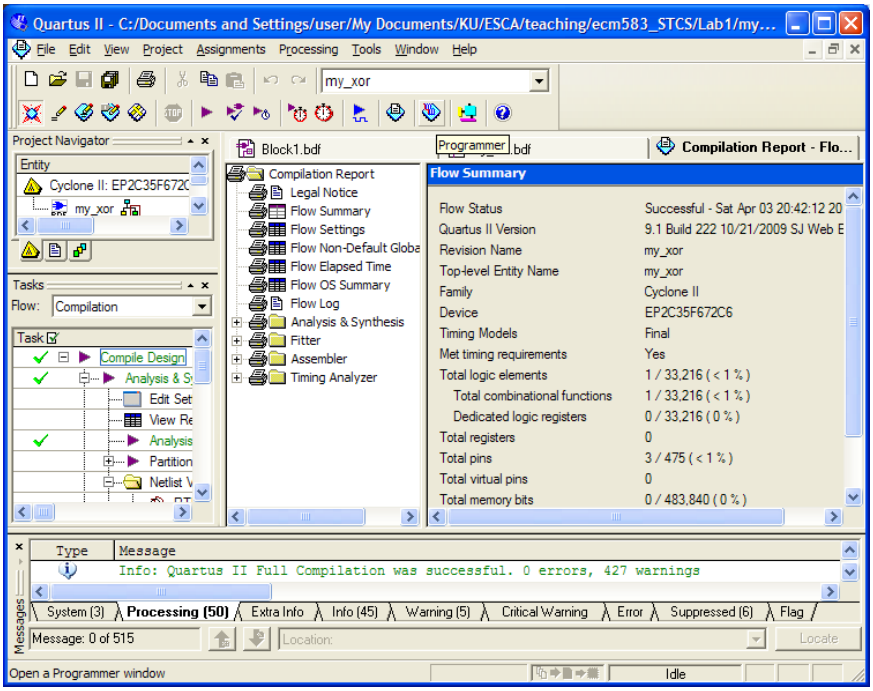
13. “Assignments” → “ Import Assignments” and import the excel file linked on the class web
    - The excel file (DE2_pin_assignments) contains pin assignment mapping



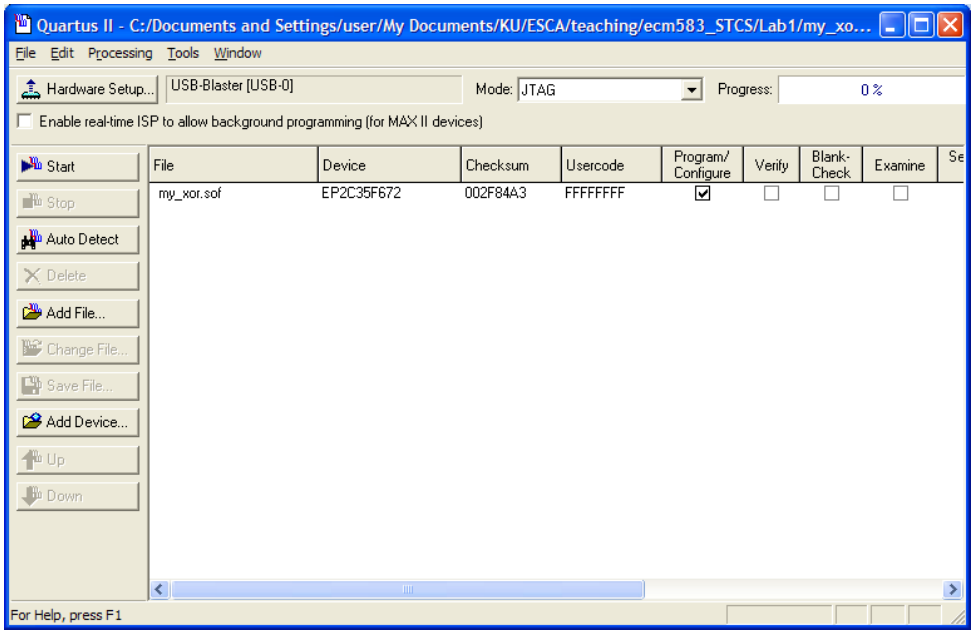
14. Ok. We are done with the design. Now double-click on “Compile Design” in the Tasks pane



15. Download your design (my_xor) to the Cyclone-II FPGA on DE2 board by clicking on “Programmer”

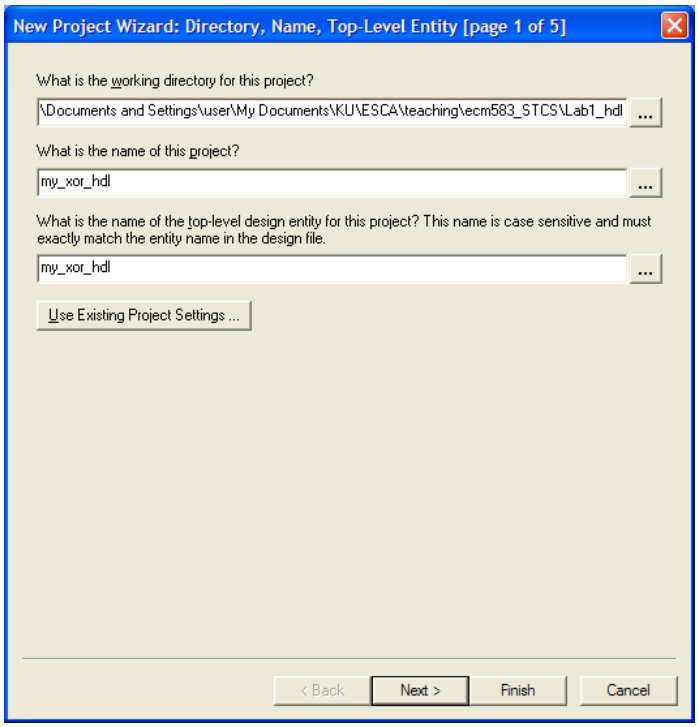


16. Click on “Start”. Now test your XOR by pushing the keys on the DE2 board.

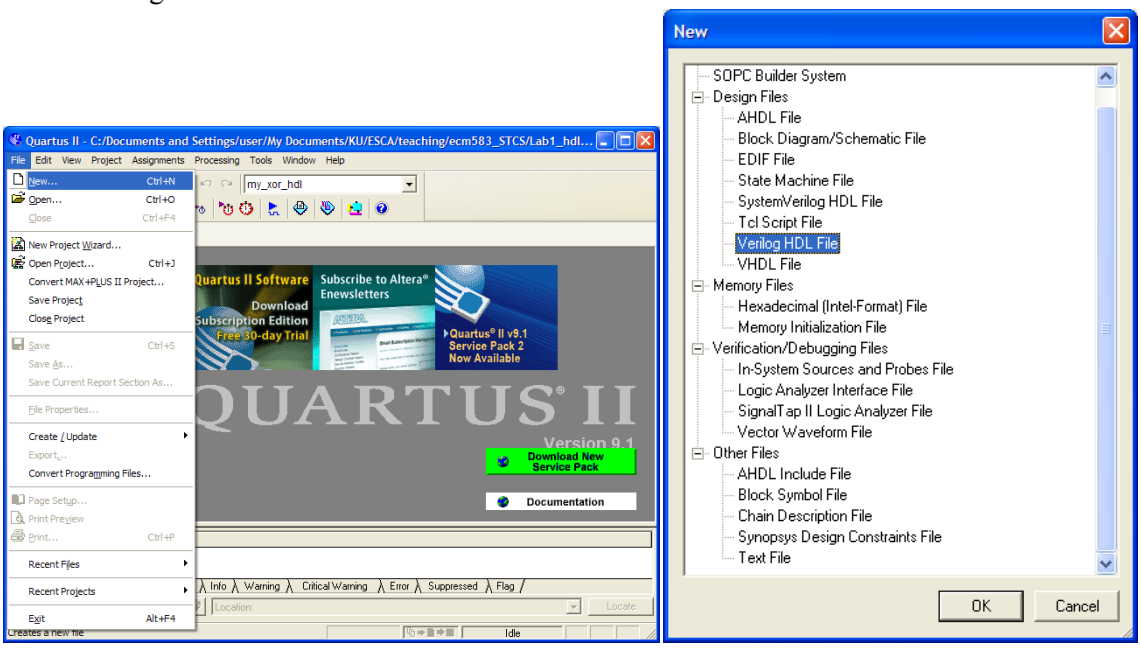


2. HDL-Based Design

1. Follow the same steps from step 1 to step 4 as in Schematic-based design.
    - But in this case, we create another directory called “Lab1_hdl” and put the project name to “my_xor_hdl” as shown below.



2. File → New
3. Choose “Verilog HDL File”



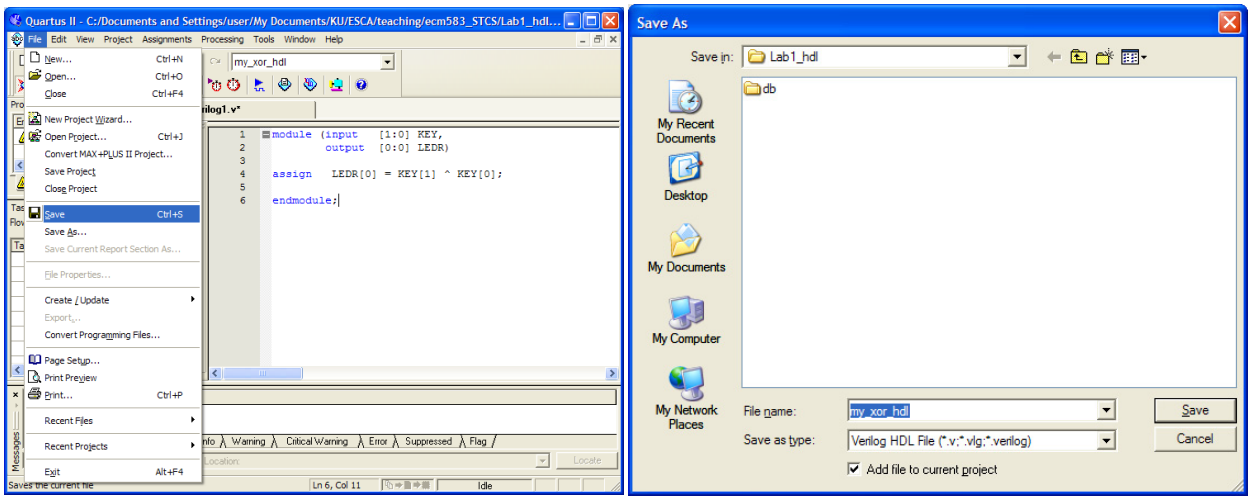
4. Copy the following code as shown below.

```
module my_xor_hdl (input  [1:0] KEY,
                   output [0:0] LEDR);

assign LEDR[0] = KEY[1] ^ KEY[0];

endmodule
```

5. “File” → “Save”, put “my_xor_hdl” in the File name, and click on “Save”



6. Follow the same steps from the step 13 to the end in Schematic-based design